

Compal Confidential
EH7LW/EH5LW/FH5TW/EH7LC/EH5LC
UMA MB Schematic Document
LA-H792P
Rev: 2.0
2019.05.29

| | | | | | |
|---|------------|--------------------|------------|--------------------------|--------------------|
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| | | | | Custom | EH7LW M/B LA-H792P |
| Date: Thursday, June 06, 2019 | | | | Sheet | 1 of 46 |
| | | | | Rev | 0.1 |

HDMI Conn.



page 29

DDI2
HDMI x 4 lanes

eDP



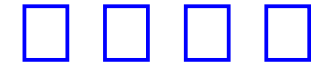
page 28

eDP

DDI

Interleaved Memory

DDR4-ON BOARD 4G 8Gb x16



page 19

260pin DDR4-SO-DIMM X1



page 20

Memory BUS
Dual Channel

1.2V DDR4 2400

USB 3.0 conn x1
USB3 port 1
USB2 port 1

USB 2.0 conn x2
USB2 port2 (MB)Camera
USB2 port4(SUB)USB2 port 7

CMOS



page 35



page 35



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Card Reader
RTS5140
Reserved

USB2 port 6(SUB)

Finger Printer
USB2 port 5

USBx8 48MHz

HD Audio 3.3V 24MHz

SPI

SPI ROM
128Mb page 9

HDA Codec
ALC255 page 32

Touch Screen

USB2 port 3 page 28

Int. Speaker

page 32

Int. DMIC on Camera

page 28

UAI

page 35



Intel Whiskey lake U
Intel Comet lake U

Processor

Cannon Lake PCH-LP

46x24 mm

15W

1528pin BGA
page 07~18

WHL-U 4+2
WHL-U 2+2

LPC/eSPI BUS

CLK=24MHz

ENE
KB9022 page 36

Int.KBD



page 37

Touch Pad
PS2 (from EC) / I2C (from SOC)
USB2 port 8 (FP)



page 37

SATA Gen 3 6.0 Gb/s (SATA2)
PCIe 3.0 x4 8GT/s Port 9-12
Flexible IO Base-U PCIe 3.0x2 (CML)

NGFF
WLAN
support CNVi
USB2 port 10



PCIe 1.0 2.5GT/s
port 6 page 31

LAN(GbE)
Realtek 8111H
page 30

RJ45 conn.



SATA HDD
Conn.



page 33

SATA ODD
Conn.

Sub Board

LS-H802P
HDD/B
page 26

LS-H783P
LID/B
page 31

LS-H781P
IO/B
page 31

LS-H784P
ODD/B
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Fan Control
page 32

RTC CKT.
page 15

Power On/Off CKT.
page 30

DC/DC Interface CKT.
page 33

Power Circuit DC/DC
page 34~43

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| Issued Date | 2018/12/27 | Deciphered Date | 2019/12/27 | Block Diagrams | |
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| | | | | Date: Thursday, June 06, 2019 | Rev 0.1 |
| | | | | Sheet 2 of 46 | |

| Vcc | 3.3V +/- 5% | | | | | |
|----------|-------------|----------------------|----------------------|----------------------|-------------|--------------|
| Ra | 100K +/- 1% | | | | | |
| Board ID | Rb | V _{BID} min | V _{BID} typ | V _{BID} max | EC AD3 | PCB Revision |
| 0 | 0 | 0 V | 0 V | 0.300 V | 0x00 - 0x13 | 0.1 (EVT) |
| 1 | 12K +/- 1% | 0.347 V | 0.345 V | 0.360 V | 0x14 - 0x1E | 0.2 (DVT) |
| 2 | 15K +/- 1% | 0.423 V | 0.430 V | 0.438 V | 0x1F - 0x25 | 0.3 (PVT) |
| 3 | 20K +/- 1% | 0.541 V | 0.550 V | 0.559 V | 0x26 - 0x30 | 1.0 (PreMP) |
| 4 | 27K +/- 1% | 0.691 V | 0.702 V | 0.713 V | 0x31 - 0x3A | |
| 5 | 33K +/- 1% | 0.807 V | 0.819 V | 0.831 V | 0x3B - 0x45 | |
| 6 | 43K +/- 1% | 0.978 V | 0.992 V | 1.006 V | 0x46 - 0x54 | |
| 7 | 56K +/- 1% | 1.169 V | 1.185 V | 1.200 V | 0x55 - 0x64 | |

| BOM Option Table | |
|---------------------|---------------|
| Item | BOM Structure |
| Unpop | @ |
| Connector | CONN@ |
| CODEC | 255@/256@ |
| EC Mode Select | LPC@ / ESPI@ |
| For Intel CMC | CMC@ |
| CNVi /BT PCM Select | CNVi@/PCM@ |
| EMI requirement | EMI@ / @EMI@ |
| ESD requirement | ESD@ / @ESD@ |
| RF requirement | @RF@ |
| TPM | TPM@ |
| Finger Print | FP@/FPFMC@ |
| Finger print power | FP3V@/FP5V@ |
| UMA or DGPU | UMA@/VGA@ |
| CPU Select | WHL@/CML@ |
| SATA/ODSelect | RD@/NRD@/ODD@ |
| USB charger | CHG@ |

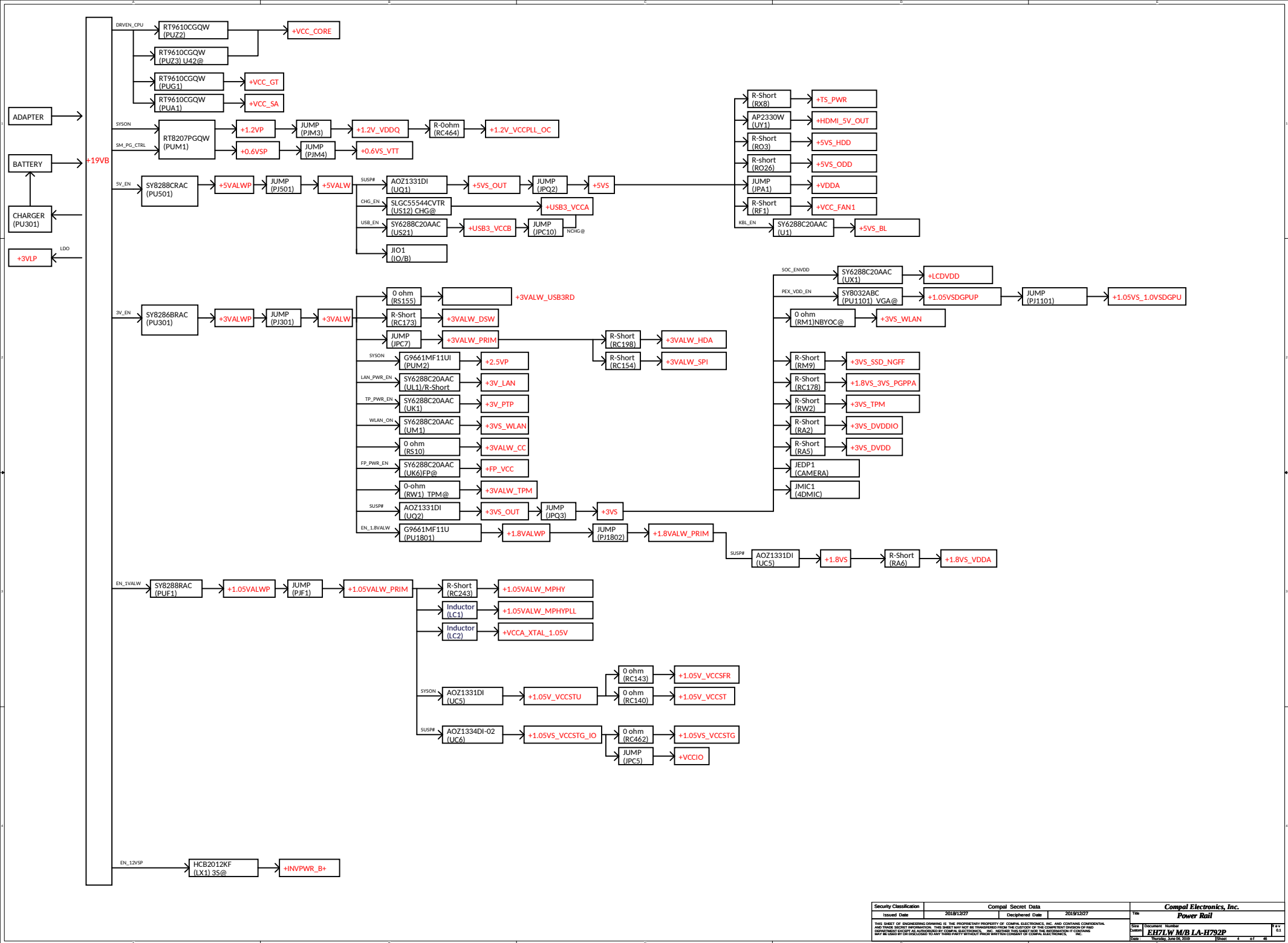
| BOM Option Table | |
|-------------------------|-------------------------------------|
| Item | BOM Structure |
| MB Stage | EVT@/DVT@/PVT@/MP |
| G Sensor | GSEN@ |
| For over 3 cell battery | B5@ |
| MD BOM Select | NOX76@/X76DSAM@ X76DMIC@/X76DHYN |
| Memory related | SPD@/DDP@/MEM@ |
| CPU C10 support | C10@ |
| BOM select | 15DIS@/15@/ |
| | |
| | |
| | |

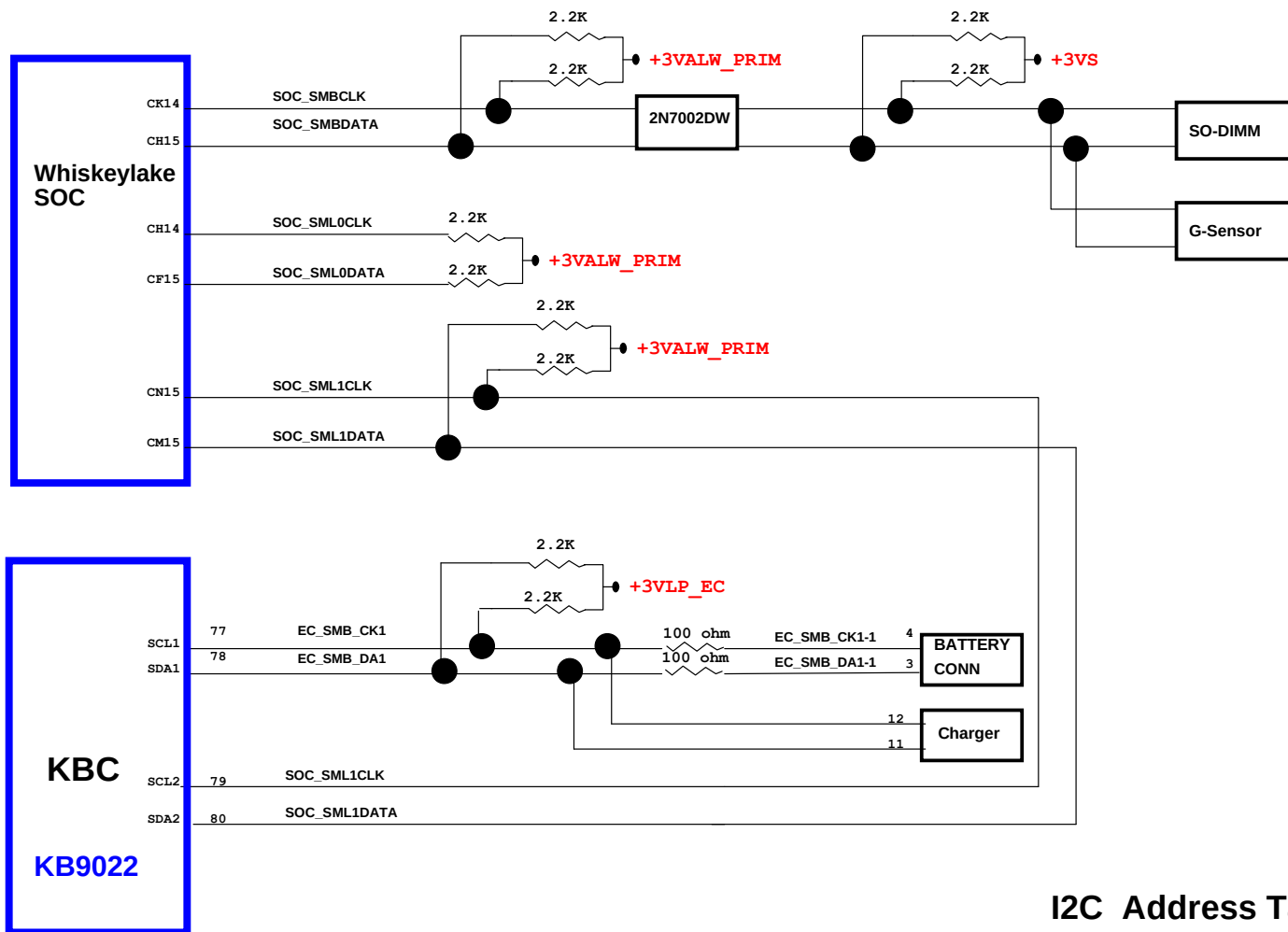
[illegible]

| SIGNAL STATE | SLP_S3# | SLP_S4# | SLP_S5# | +VALW | +V | +VS | Clock |
|----------------------|---------|---------|---------|-------|-----|-----|-------|
| S0 (Full ON) | HIGH | HIGH | HIGH | ON | ON | ON | ON |
| S3 (Suspend to RAM) | LOW | HIGH | HIGH | ON | ON | OFF | OFF |
| S4 (Suspend to Disk) | LOW | LOW | HIGH | ON | OFF | OFF | OFF |
| S5 (Soft OFF) | LOW | LOW | LOW | ON | OFF | OFF | OFF |

| Power Plane | Description | S0 | S3 | S4/S5 |
|-----------------|--|------|-----|-------|
| +19V_VIN | Adapter power supply | N/A | N/A | N/A |
| +12.6V_BATT | Battery power supply | N/A | N/A | N/A |
| +19VB | AC or battery power rail for power circuit. | N/A | N/A | N/A |
| +VCC_CORE | Processor IA Cores Power Rail | ON | OFF | OFF |
| +VCC_GT | Processor Graphics Power Rails | ON | OFF | OFF |
| +VCC_SA | System Agent power rail | ON | OFF | OFF |
| +0.6VS_VTT | DDR +0.6VS power rail for DDR terminator . | ON | OFF | OFF |
| +1.05VALW_PRIM | +1.05V Always power rail | ON | ON | ON*1 |
| +1.05V_VCCSTU | Sustain voltage for processor in Standby modes | ON | ON | OFF |
| +VCCIO | CPU IO power rail | ON | OFF | OFF |
| +1.05VS_VCCSTG | +1.0VALW_PRIM Gated version of VCCST | ON | OFF | OFF |
| +1.2V_VDDQ | DDR4 +1.2V Power Rail | ON | ON | OFF |
| +1.8VALW_PRIM | +1.8V Always power rail | ON | ON | ON*1 |
| +1.8VS | System +1.8V power rail | ON | OFF | OFF |
| +3VLP | +19VB to +3VLP power rail for suspend power | ON | ON | ON |
| +3VALW | System +3VALW always on power rail | ON | ON | ON*1 |
| +3VS | System +3V power rail | ON | OFF | OFF |
| +5VALW | +5V Always power rail | ON | ON | ON |
| +5VS | System +5V power rail | ON | OFF | OFF |
| +RTCVCC | RTC Battery Power | ON | ON | ON |
| +1.0VSDGPU | +1.0VS power rail for N17S | ON*2 | OFF | OFF |
| +1.35VSDGPU | +1.35VS power rail for GPU | ON*2 | OFF | OFF |
| +1.8VSDGPU_AON | +1.8VS power rail for N17S(AON) | ON*2 | OFF | OFF |
| +1.8VSDGPU_MAIN | +1.8VS power rail for N17S(MAIN) | ON*2 | OFF | OFF |
| +VGA_CORE | Core power for discrete GPU | ON*2 | OFF | OFF |
| | | | | |
| | | | | |
| | | | | |

Note : ON*1 means power plane is ON only when WOL enable and RTC wake at BIOS setting, otherwise it is OFF.
ON*2 power plane is ON when DGPU turn on

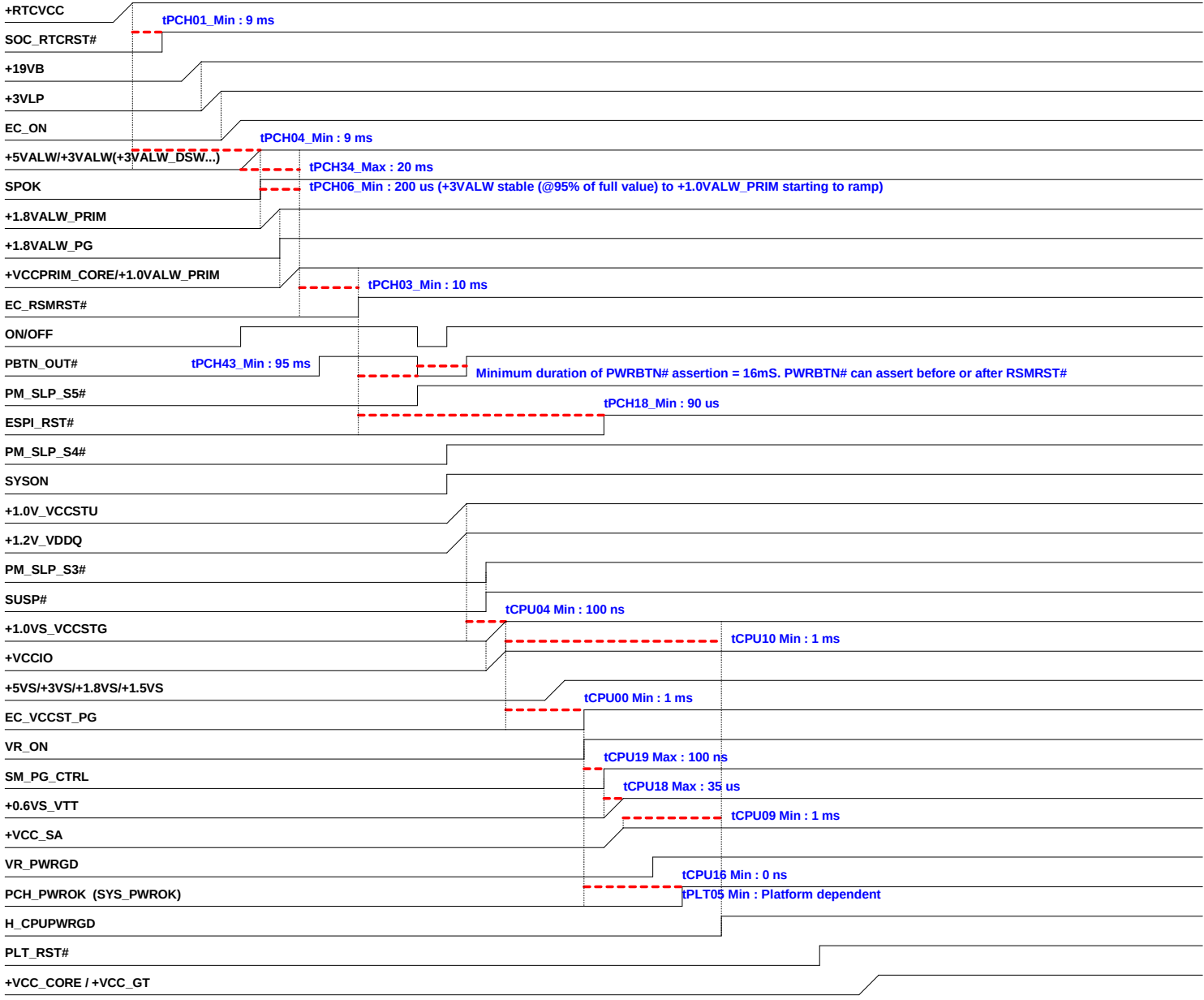




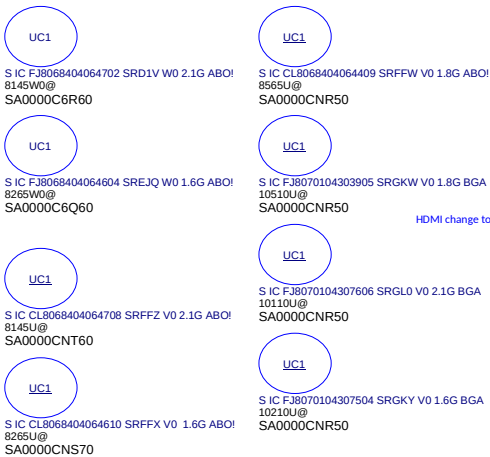
I2C Address Table

| BUS | Device | Address (8 bit) |
|---------------------------|-----------------------|-----------------|
| I2C_0 (+3VS) | Reserved | |
| I2C_1 (+3VALW_PRIM) | TM-P3393-003 (TP) | 0x2C |
| | FA577E-1206 (TP-ELAN) | 0x15 |
| | SA577C-12A0 (TP-ELAN) | 0x15 |
| SOC_SMBCLK (+3VS) | SO-DIMM2 | 0xA4 |
| | G-Sensor | 0x30 |
| SOC_SML1CLK (+3VALW_PRIM) | EC | |
| | | |
| EC_SMB_CK1 (+3VLP) | BQ24781 (Charger IC) | 0x12 |
| | BATTERY PACK | 0x16 |

PWR Sequence_SKL-U2+2_DDR3L_Value_NON CS



| | | | | | |
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| Size | | Document Number | | Rev | |
| Custom | | EH7LWM/B LA-H792P | | 0.1 | |
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HDMI change to DDI2 port 11/26

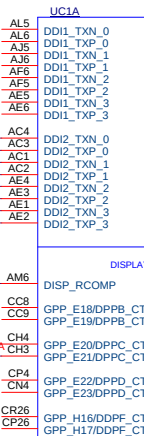
HDMI

HDMI DDC (Port B)

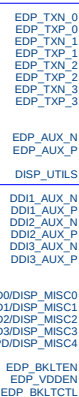
<22> SOC_DP2_CTRL_CLK
<22> SOC_DP2_CTRL_DATA

EDP_COMP

SOC_DP2_CTRL_CLK
SOC_DP2_CTRL_DATA



EDP

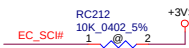


eDP

From HDMI

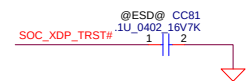
From eDP

12/21 PU

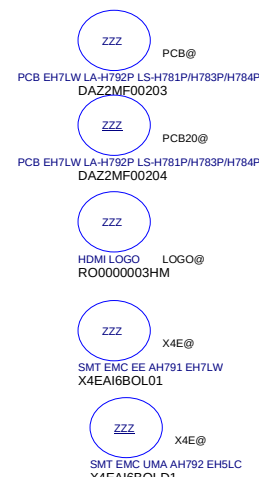
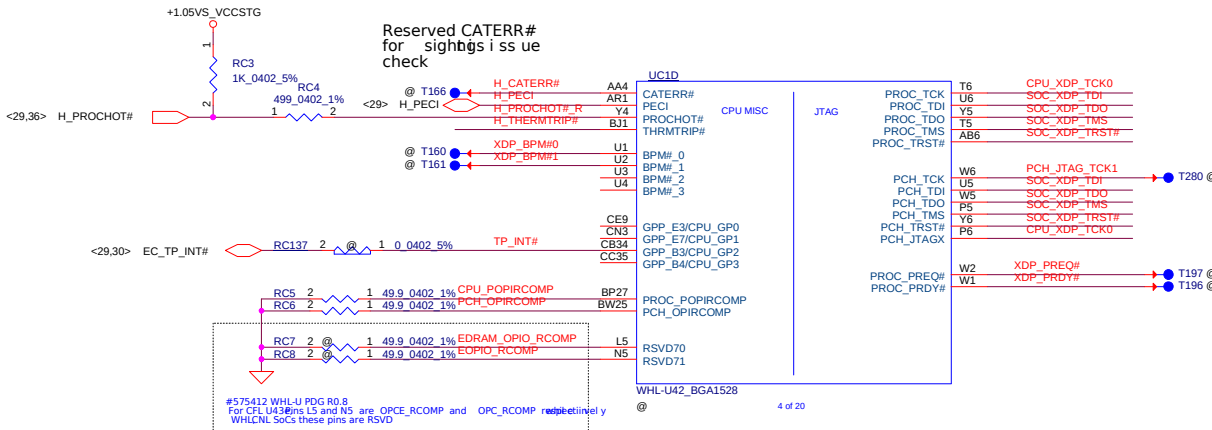
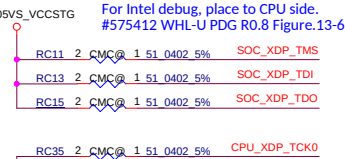
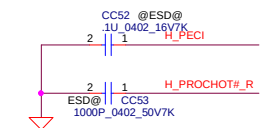
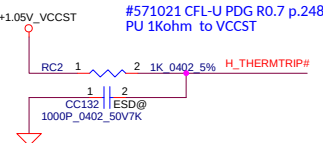


EC_SCI# SOC internal PU

#545659 PCH EDS1.51 P.131
SCI capability is available on all GPIOs, while NMI and SMI capability is available on only select GPIOs.
Below are the PCH GPIOs that can be routed to generate SMI# or NMI:
• GPP_B14, GPP_B20, GPP_B23
• GPP_C_23 : 22
• GPP_D_4 : 0
• GPP_E_8 : 0 , GPP_E_16 : 13

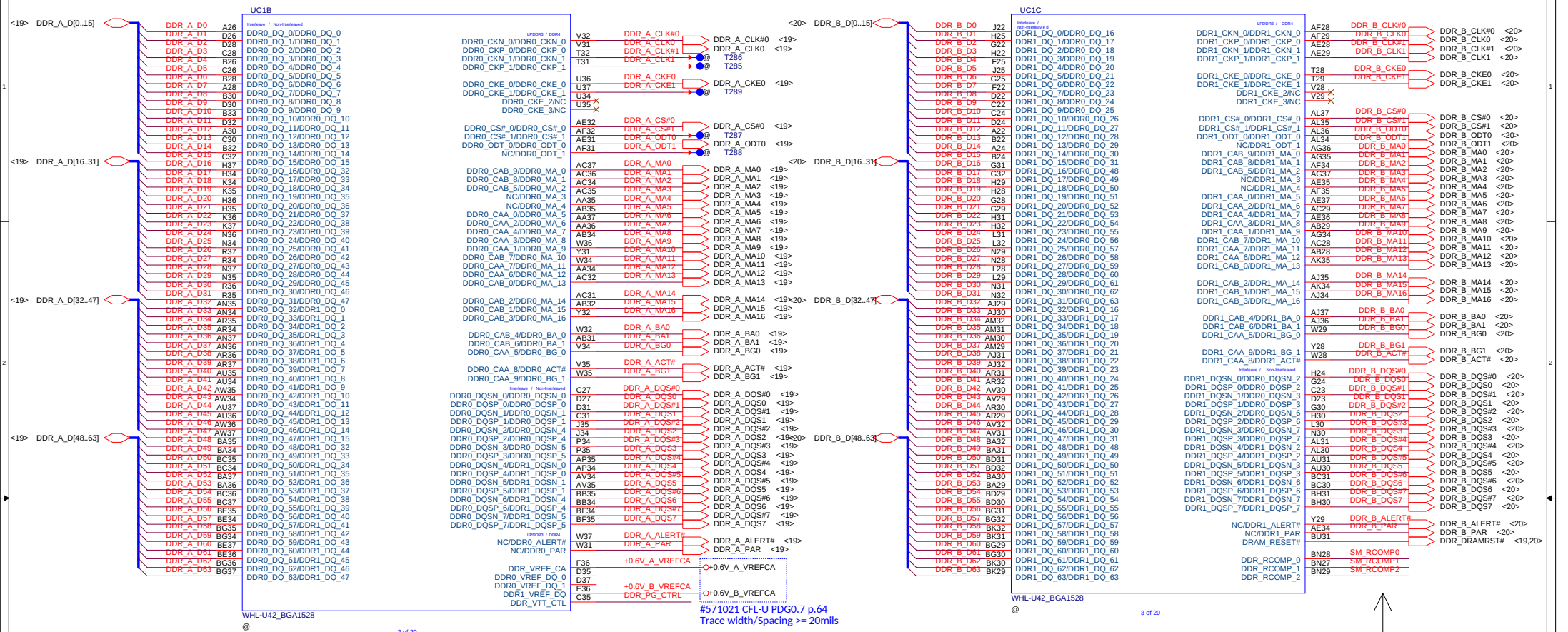


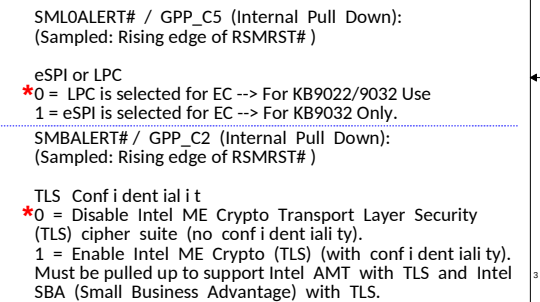
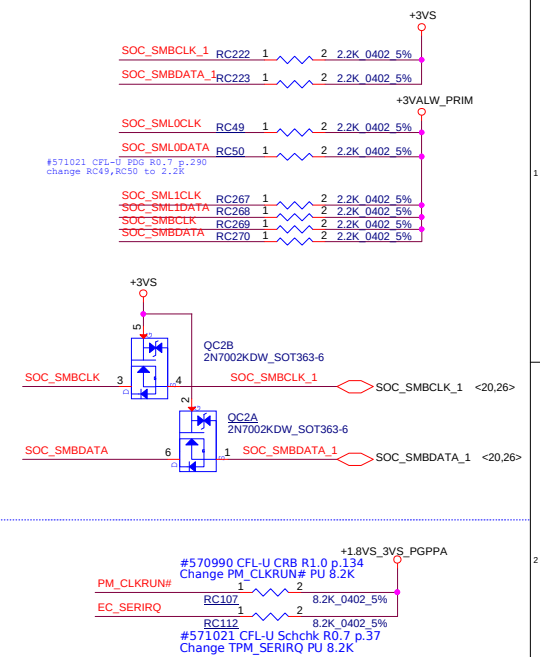
#571021 CFL-U PDG R0.7 p.39
PU 24.9ohm for eDP



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| | | | | Date Friday, August 02, 2019 | Sheet 7 of 146 |

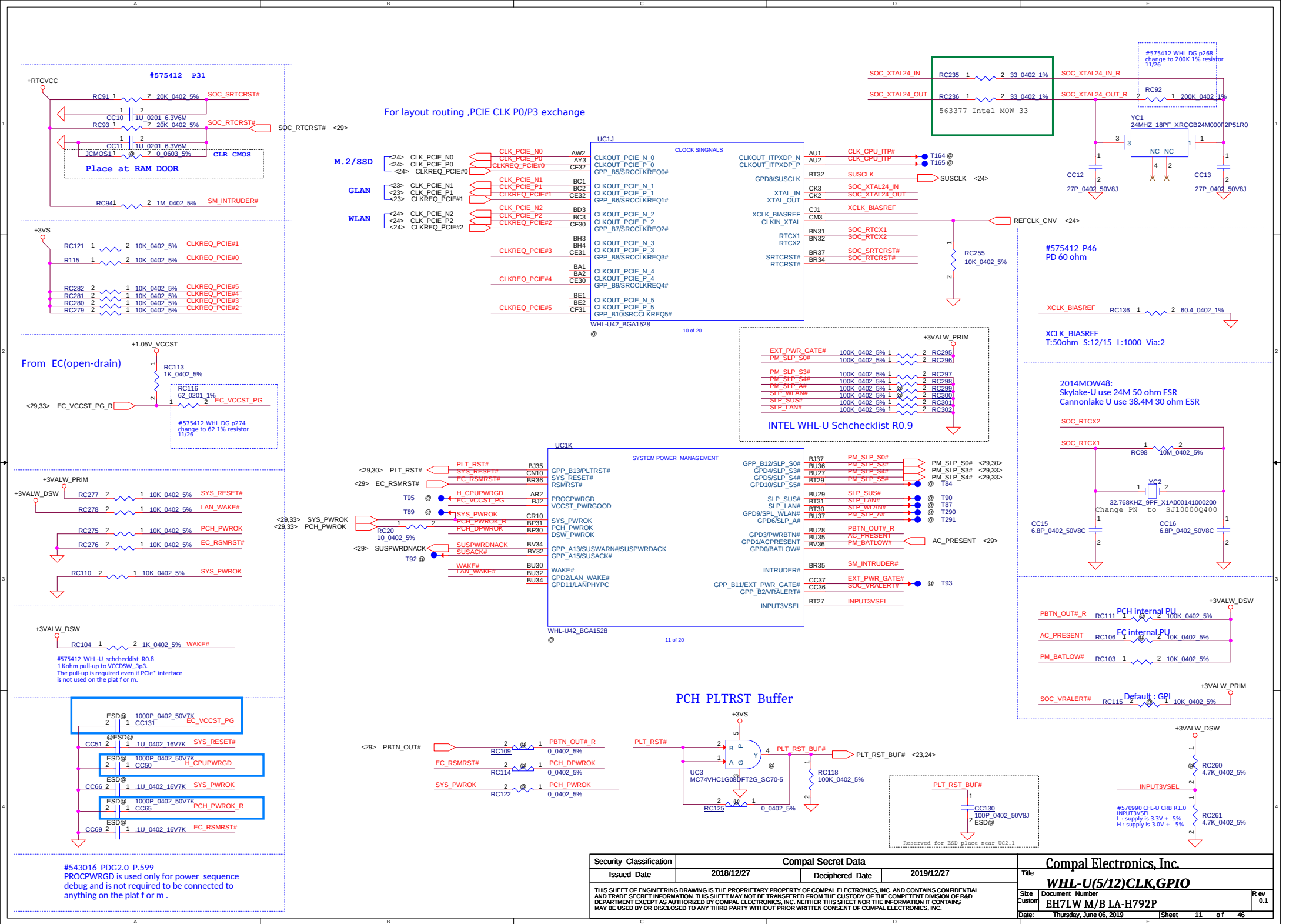
Interleaved Memory

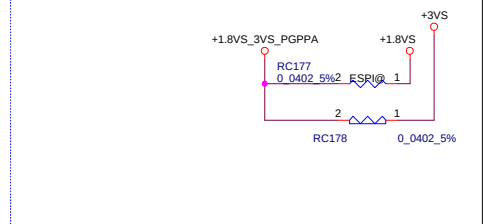
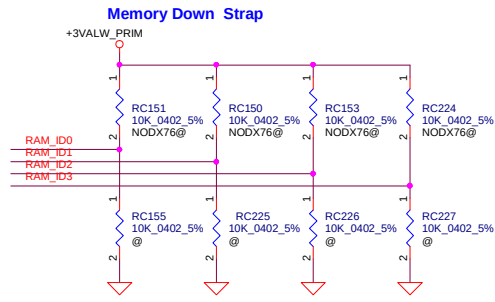
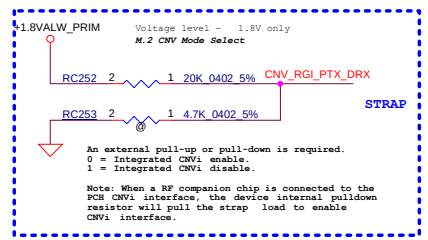
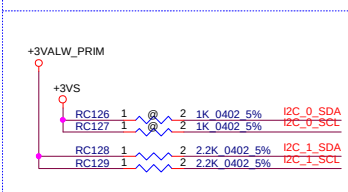
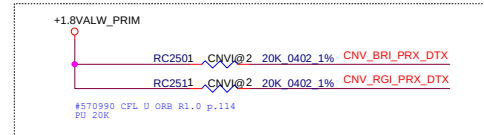
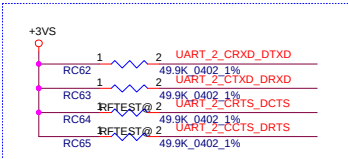
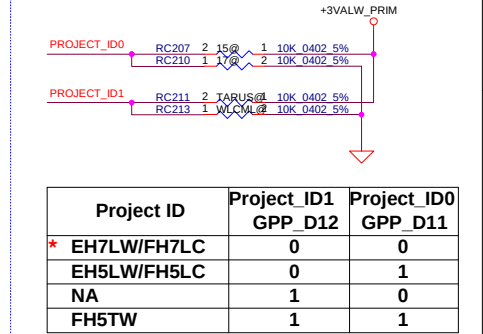
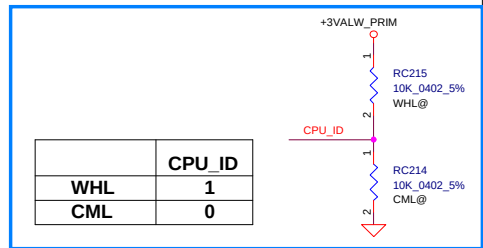
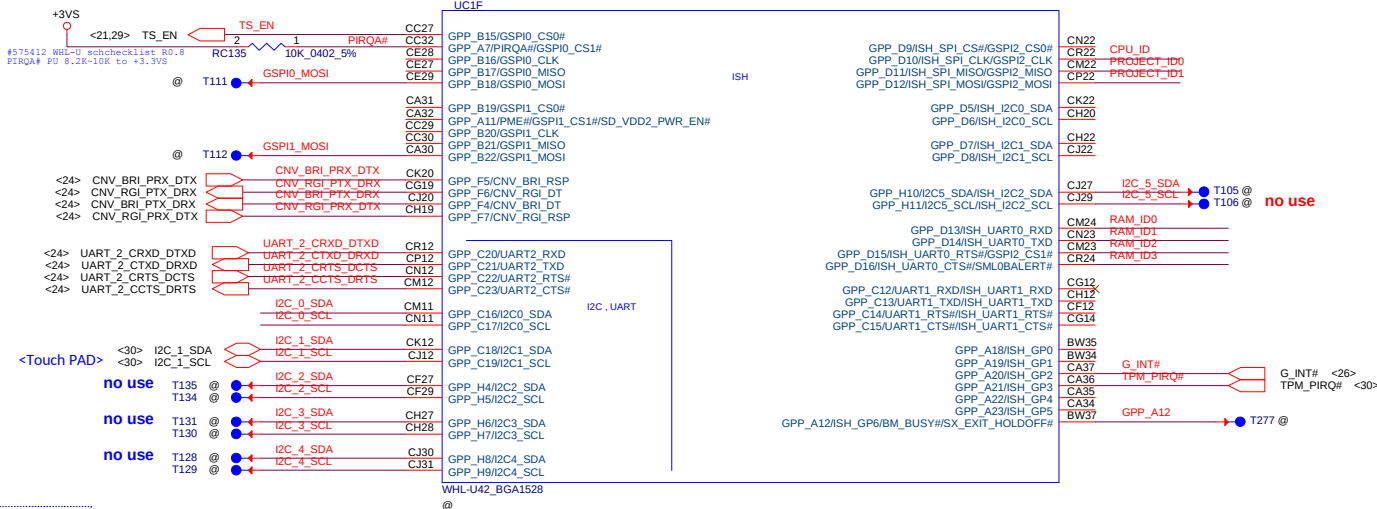




| A | B | C | D | E |
|---|---|---|---|--|
| | | | | Date: Thursday, June 06, 2019 Sheet: 9 of 40 |

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| Size | Document Number | Rev | |
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| Date: | Thursday, June 06, 2019 | Sheet | 10 of 46 |





Functional Strap Definitions

GSPiO_MOSI /GPP_B18 (Internal Pull Down):
(Rising edge of PCH_PWROK)
No Reboot

*0 = Disable No Reboot mode. --> AAX05 Use
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

GSPi1_MOSI / GPP_B22 (Internal Pull Down):
(Rising edge of PCH_PWROK)

Boot BIOS Strap Bit
*0 = SPI Mode --> AAX05 Use
1 = LPC Mode

- ZZZ1 Hynix4GB X76DHYN@ X76829BOL04
- ZZZ2 Micron4GB X76DMIC@ X76829BOL05
- ZZZ3 Samsung4GB X76DSAM@ X76829BOL06

| | RAM_ID3 | RAM_ID2 | *RAM_ID1 | *RAM_ID0 | PartNumber - Description |
|-------------------|---------|---------|----------|----------|--|
| Hynix 4GB | 0 | 0 | 0 | 0 | SA0000BMN30 (S IC D4 512M16 H5AN8G6NCJR-VKC FBGA ABO!) |
| Micron 4GB | 0 | 0 | 0 | 1 | SA0000ARD60 (S IC D4 8G/2666 MT40A512M16LY-075:E ABO!) |
| Samsung 4GB | 0 | 0 | 1 | 0 | SA0000B6F00 (S IC D4 512M16 K4A8G165WC-BCTD FBGA 96P) |
| | 0 | 0 | 1 | 1 | |
| No OnBoard Memory | 1 | 1 | 1 | 1 | No On Board Memory |

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| | | | | Size | Rev |
| | | | | Customer | 0.1 |
| | | | | Date | Thursday, June 06, 2019 |
| | | | | Sheet | 12 of 46 |

11/28
For layout routing
PCIE P5/P6 exchange

NGFF WLAN+BT (Key E)

GLAN

HDD

ODD

NGFF SSD (Key M)
(Need Lane Reversal)

* CML Base not support SATA founcti
#575412 p.46
PCIE_RCOMP/PN/PCIE_RCOMP
R=100ohm

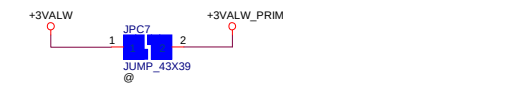
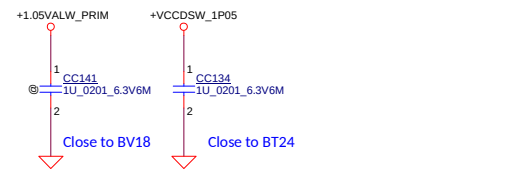
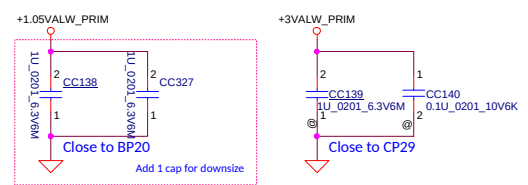
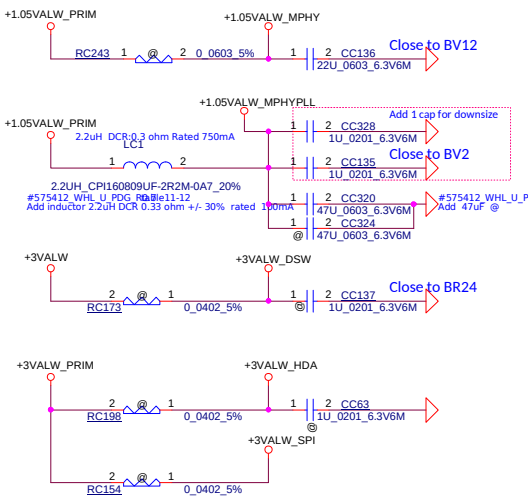
6.1.2.1 Cannon Lake U (CNL U) PCH-LP

Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL U PCH-LP

| Flex I/O Lane | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|-------------------------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------|---------|---------|----------|----------|----------|----------|----------|----------|----------|
| High Speed I/O (HSIO) Type and Lane | USB3.1 Gen1/Gen2 #1 | USB3.1 Gen1/Gen2 #2 | USB3.1 Gen1/Gen2 #3 | USB3.1 Gen1/Gen2 #4 | USB3.1 Gen1/Gen2 #5 | USB3.1 Gen1/Gen2 #6 | PCIe #7 | PCIe #8 | PCIe #9 | PCIe #10 | PCIe #11 | PCIe #12 | PCIe #13 | PCIe #14 | PCIe #15 | PCIe #16 |
| Intel® RST Support | No Support | No Support | No Support | No Support | No Support | No Support | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |

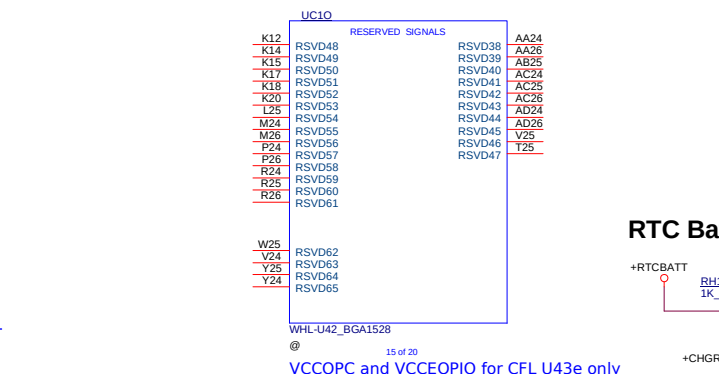
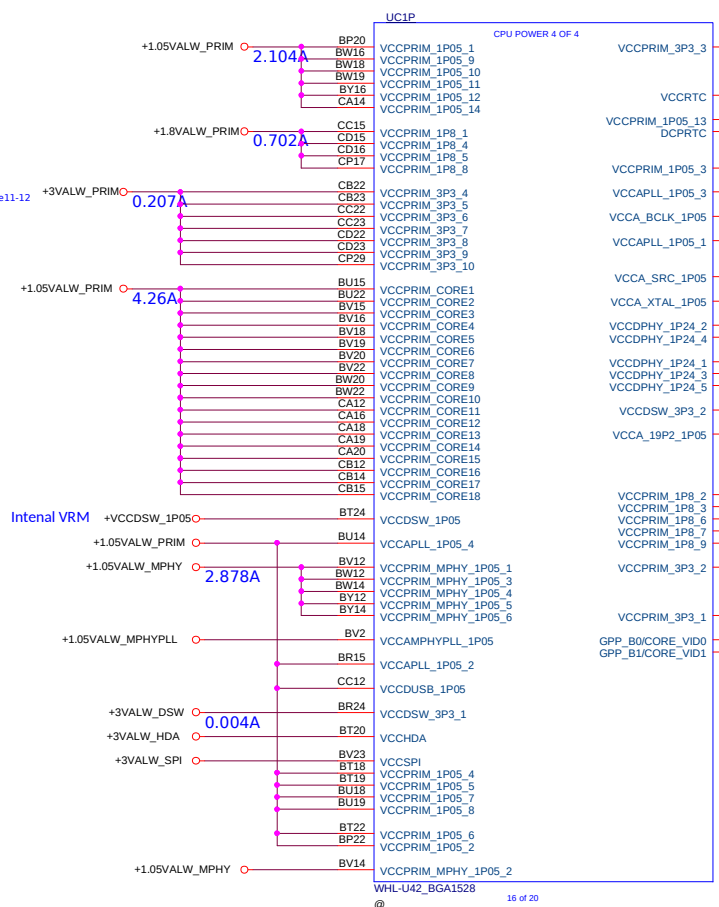
| GPIO | DEVICE CONTROL |
|----------|----------------|
| USB_OC0# | USB2 Port 1 |
| USB_OC1# | NA |
| USB_OC2# | NA |
| USB_OC3# | NA |
| DEVSLP0 | NA |
| DEVSLP1 | NA |
| DEVSLP2 | NA |
| SATA_GP0 | NA |
| SATA_GP1 | NA |
| SATA_GP2 | NA |

| Security Classification | Compal Secret Data | Title |
|--|--------------------|---|
| Issued Date | 2018/12/27 | Deciphered Date |
| 2019/12/27 | | |
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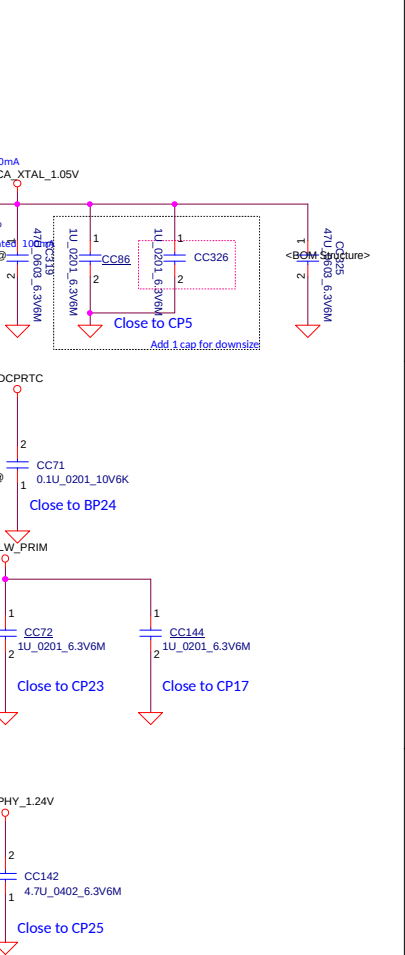
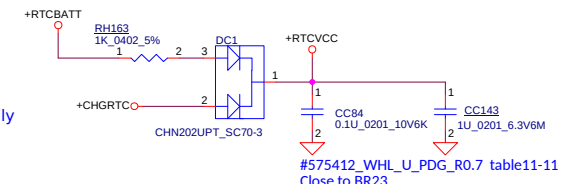


#543016 PDG2.0 P.470
VCCRTC does not exceed 3.2 V.

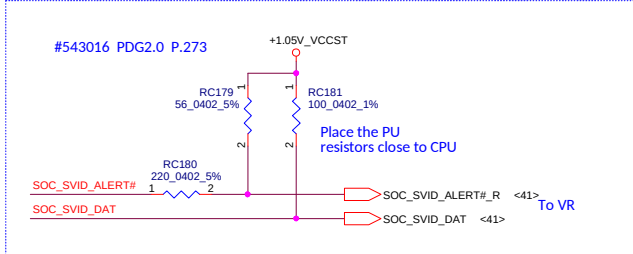
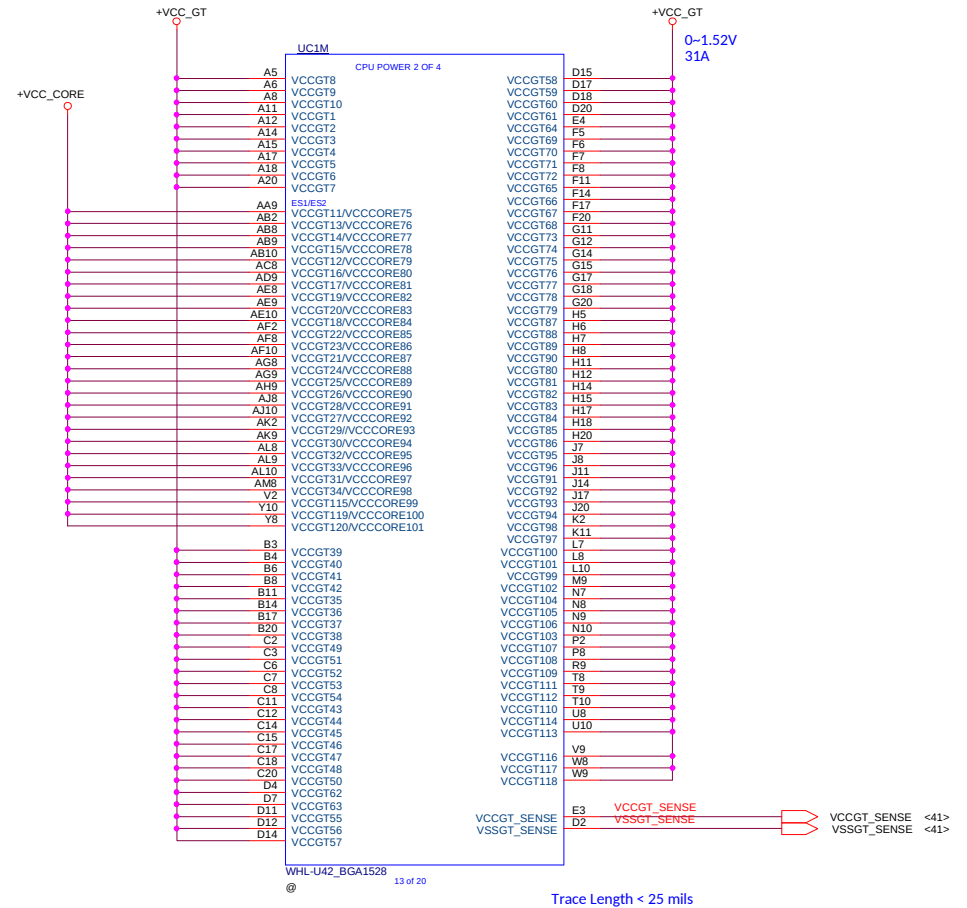
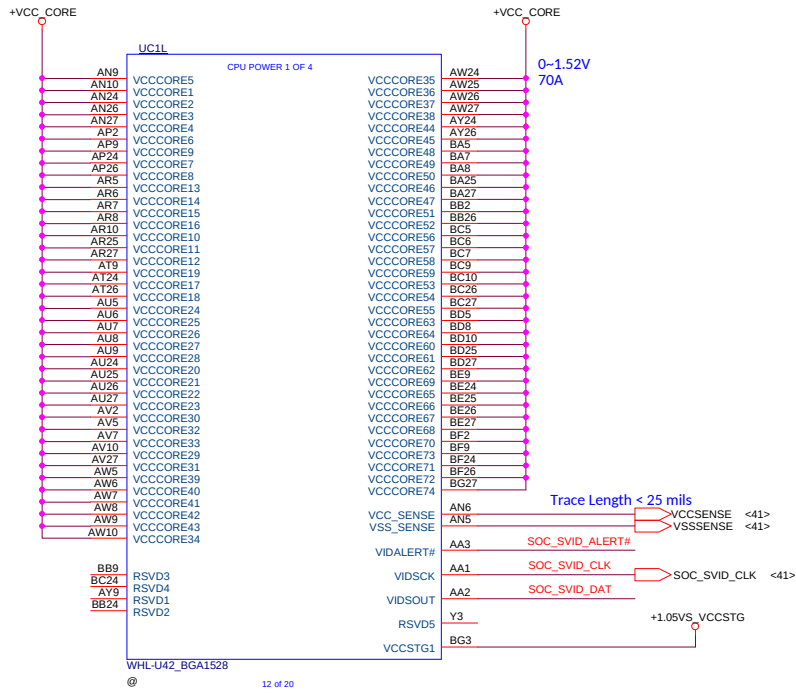
| Power Rail | Voltage |
|---------------|-------------|
| +CHGRTC | 3.383V(MAX) |
| BAT54C(VF) | 240 mV |
| +RTCVCC | 3.143V |
| Result : Pass | |



RTC Battery

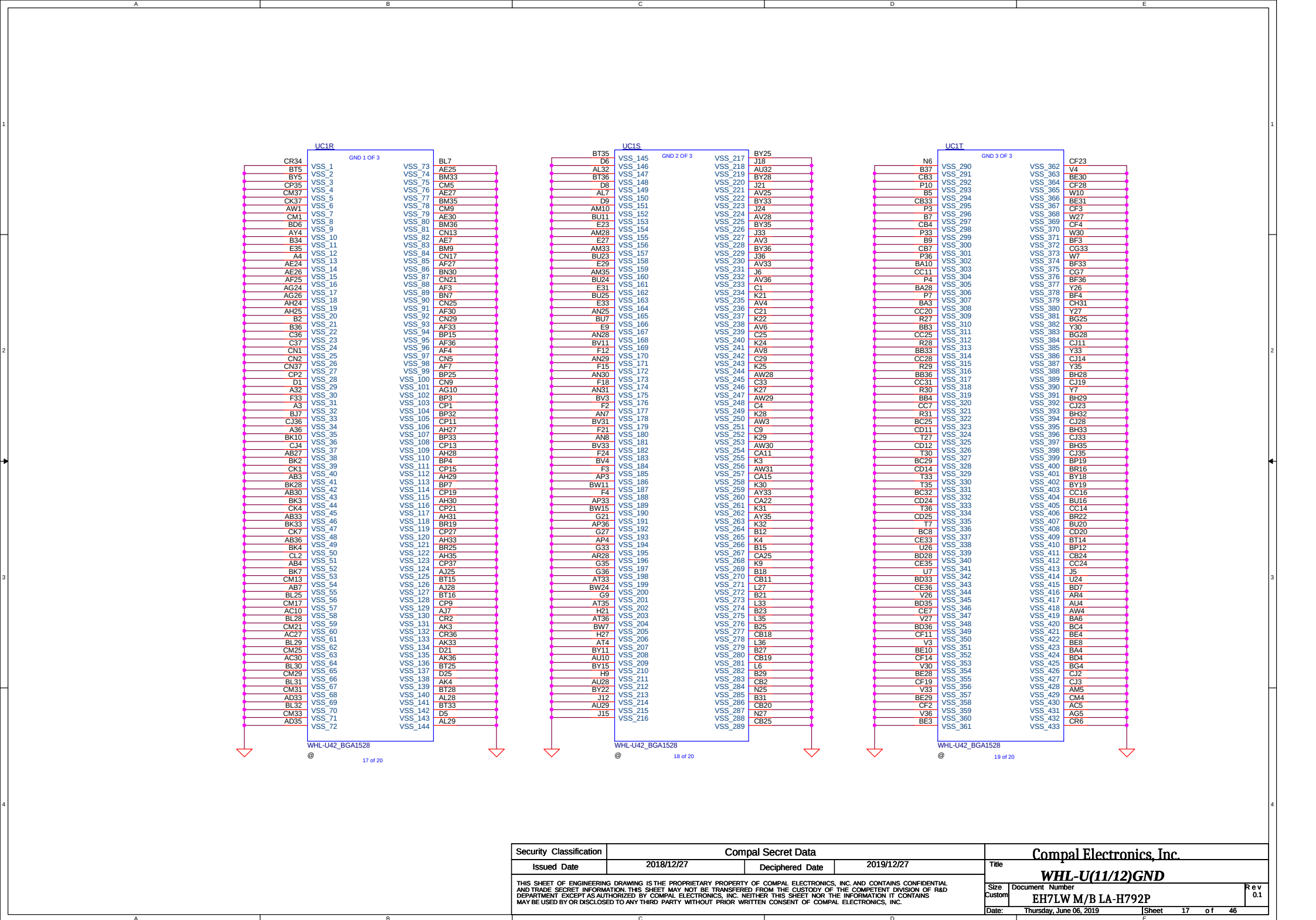


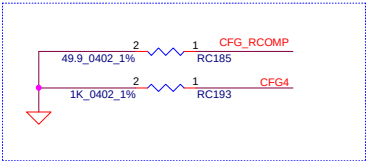
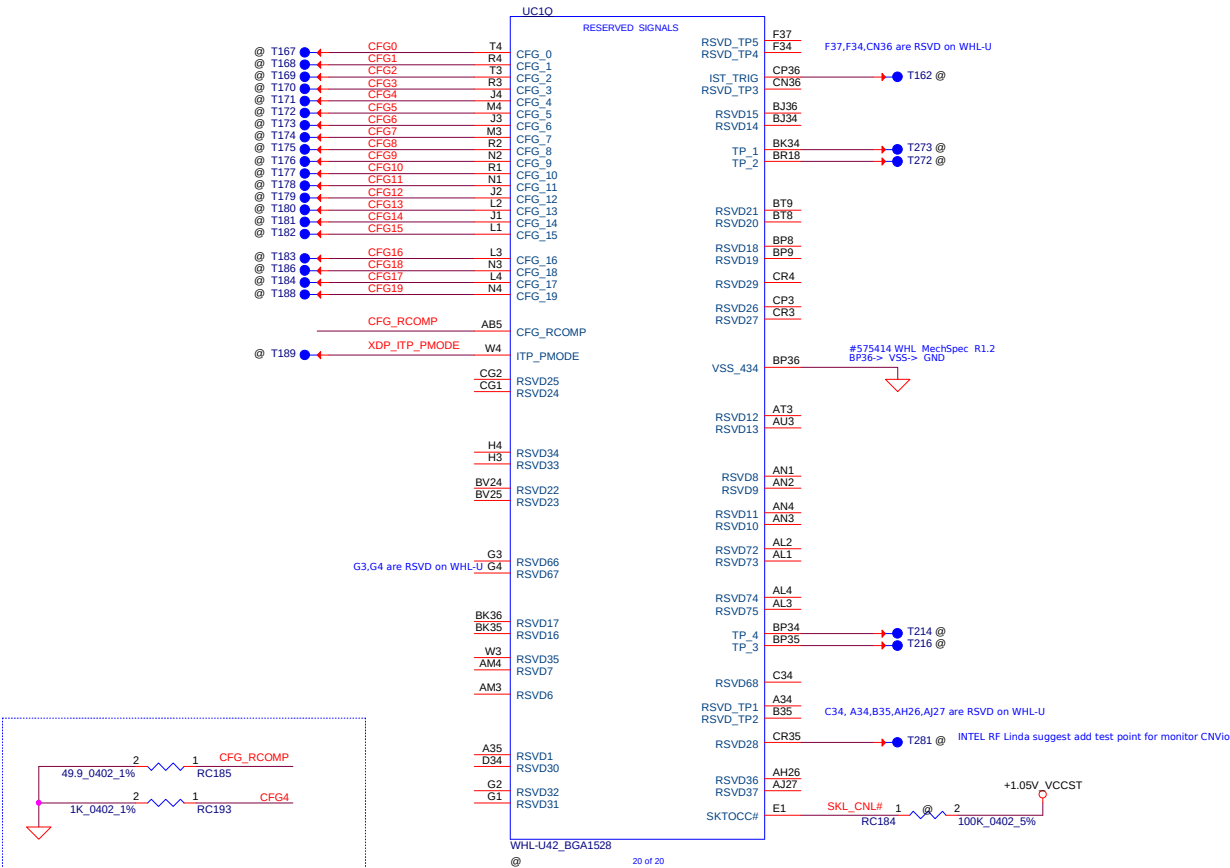
| Security Classification | Compal Secret Data | | | Title | |
|---|--------------------|-----------------|------------|-------------------------------|----------------|
| Issued Date | 2018/12/27 | Deciphered Date | 2019/12/27 | WHL-U(9/12)Power | |
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| | | | | EH7LW M/B LA-H792P | 0.1 |
| | | | | Date: Thursday, June 06, 2019 | Sheet 15 of 46 |



Processor Power Rails

| Power Rail | Description | Control |
|------------------------|---|-------------------------------------|
| V _{CC} | Processor IA Cores Power Rail | SVID |
| V _{CCGT} | Processor Graphics Power Rails | SVID |
| V _{CCGTx} | Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs | SVID |
| V _{CCSA} | System Agent Power Rail | SVID/Fixed (SKU dependent) |
| V _{CCIO} | IO Power Rail | Fixed |
| V _{CCST} | Sustain Power Rail | Fixed |
| V _{CCPLL} | Processor PLLs power rail | Fixed |
| V _{DDQ} | Integrated Memory Controller Power Rail | Fixed (Memory technology dependent) |
| V _{CCOPC} | Processor OPC power rail (available only in SKU's with OPC) | Fixed |
| V _{CCOPC_1P8} | Processor OPC power rail (available only in SKU's with OPC) | Fixed |
| V _{CCEDPIO} | Processor EDPPIO power rail (available only in SKU's with OPC) | Fixed |





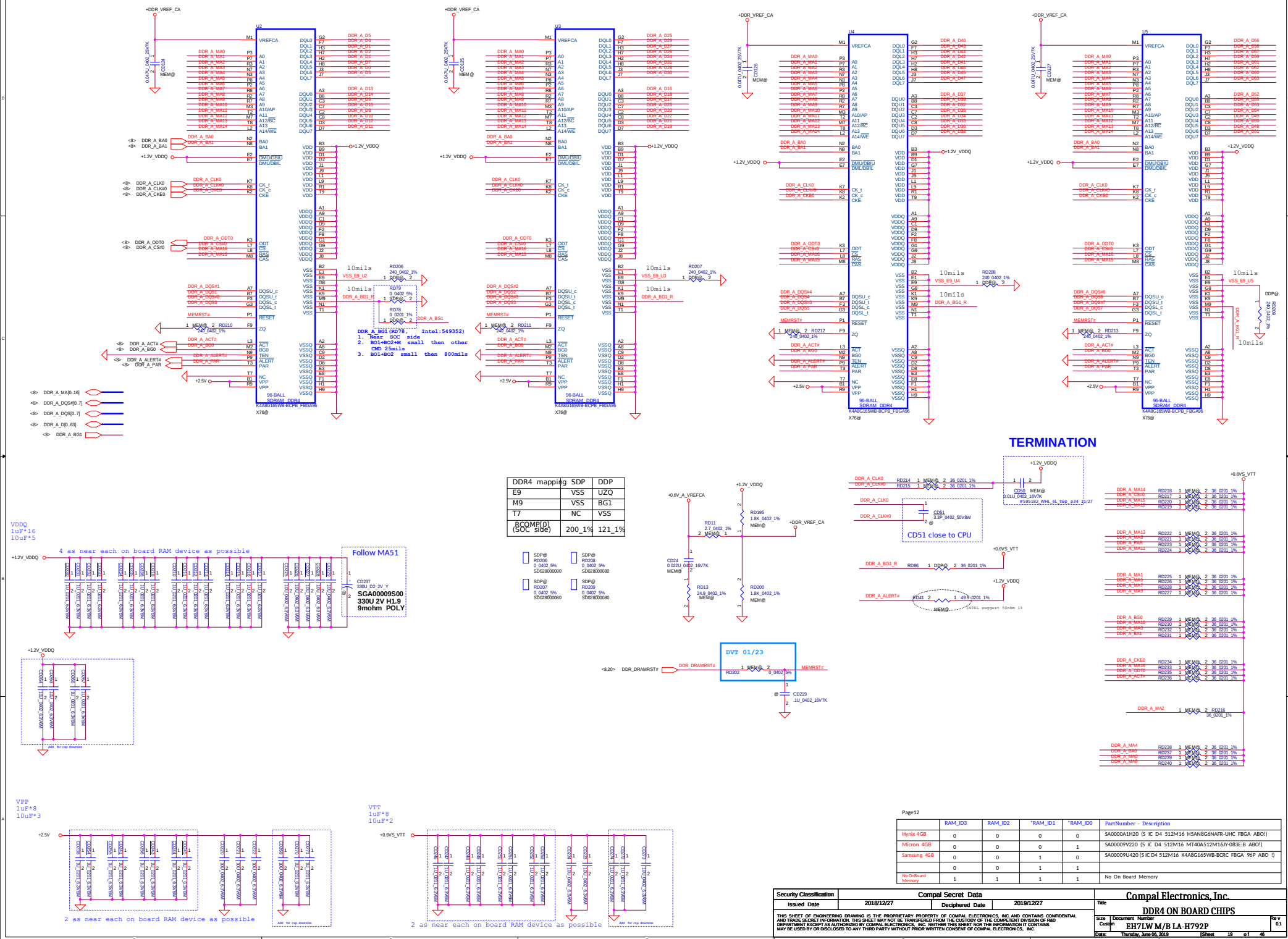
Display Port Presence Strap

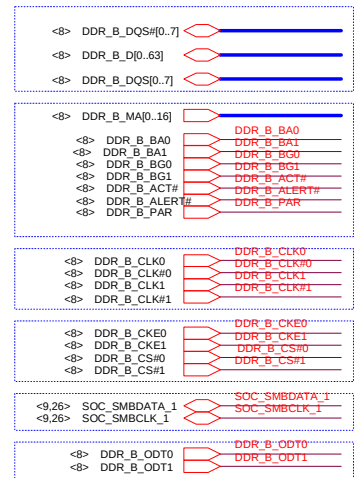
CFG4

1 : Disabled; No Physical Display Port
at t a c h e d t o E m b e d d e d D i s p l a y P o r t

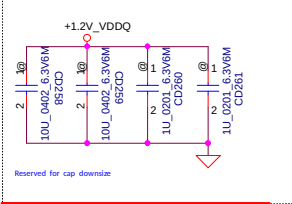
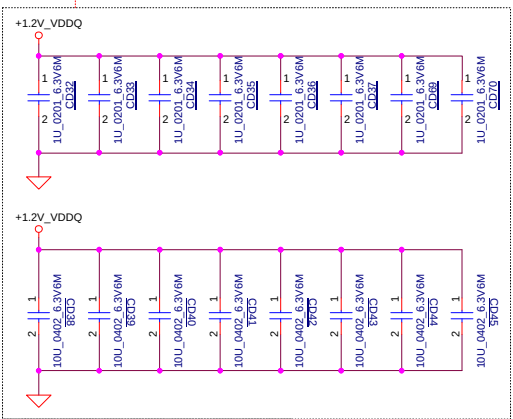
0 : Enabled; An external Display Port device is
connected to the Embedded Display Port

#544669 CRB1.1 P.54
#544924 SKL EDS1.2 P.125
PROC_SELECT#
This pin is for compatibility with future
platforms. It should be unconnected for
the processor.

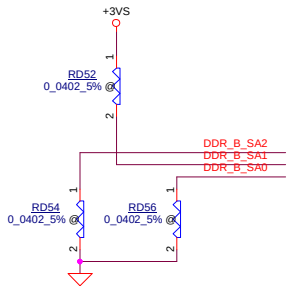
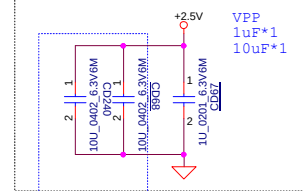




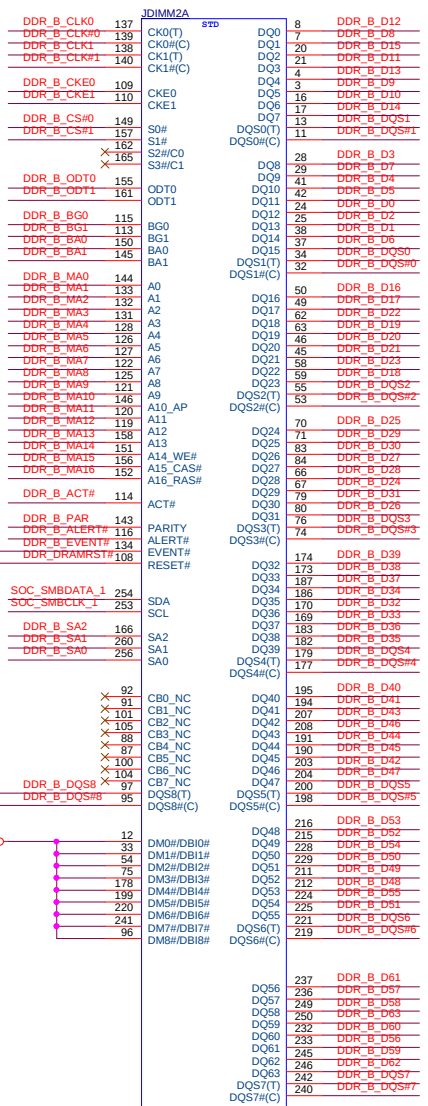
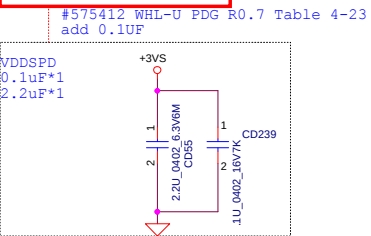
Layout Note:
Place near JDIMM2



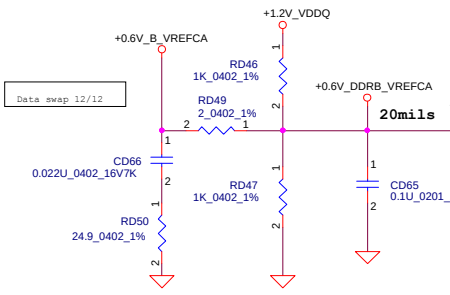
Layout Note:
Place near JDIMM1.257,259



Layout Note:
Place near JDIMM2.255

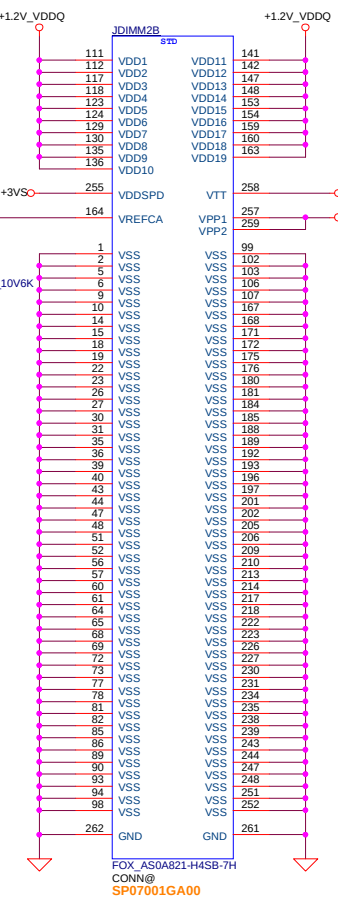


Compatible with SP07001HW00

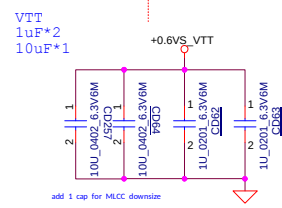


Place near to SO-DIMM connector.

Standard Type
2-3A to 1 DIMMs/channel

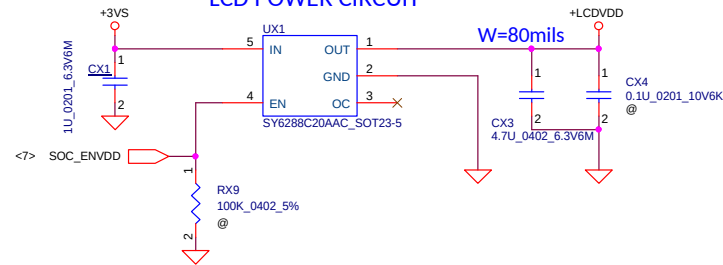


Layout Note:
Place near JDIMM1.258



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|---|------------|--------------------|------------|----------------|--------------------------------------|
| Issued Date | 2018/12/27 | Deciphered Date | 2019/12/27 | DDR4 DIMMB | |
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| | | | | Date | Thursday, June 06, 2019 |
| | | | | Sheet | 20 of 46 |

LCD POWER CIRCUIT

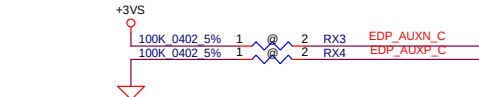
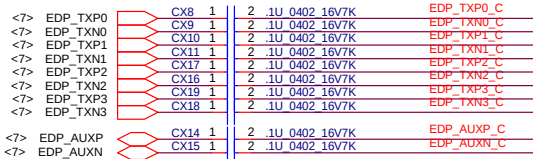
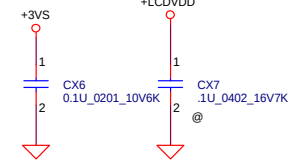


W=60mils

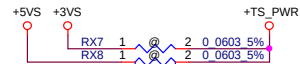
SM01000EJ00 3000ma
220ohm@100mhz
DCR 0.04

Note: Unmount LX1 when panel boost circuit was use. (2S battery cell)

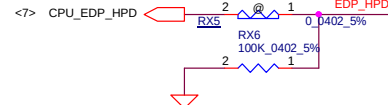
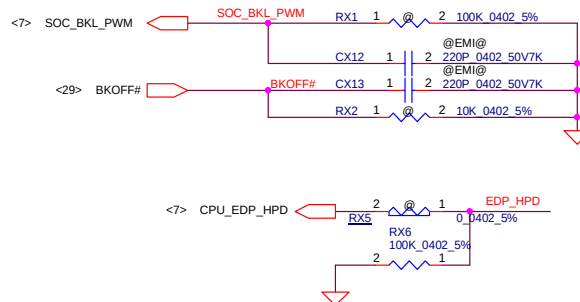
Place closed to JEDP1



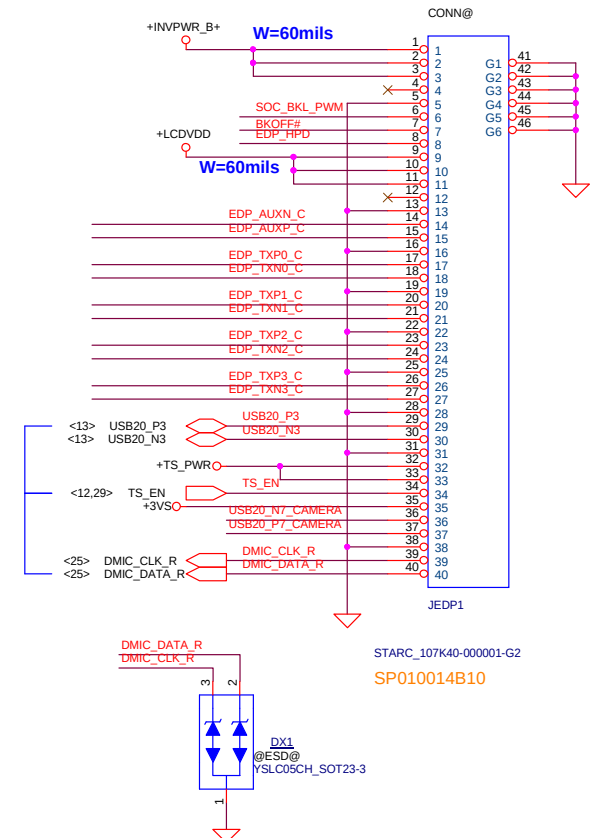
Touch Screen



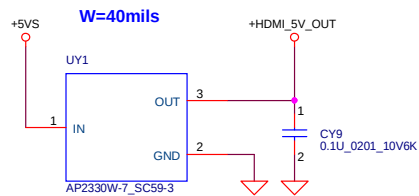
Camera



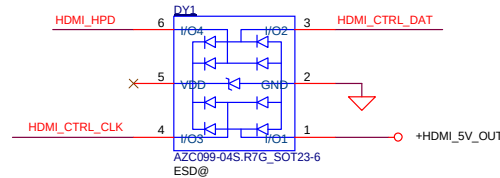
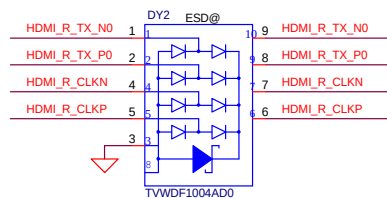
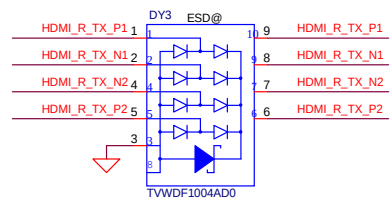
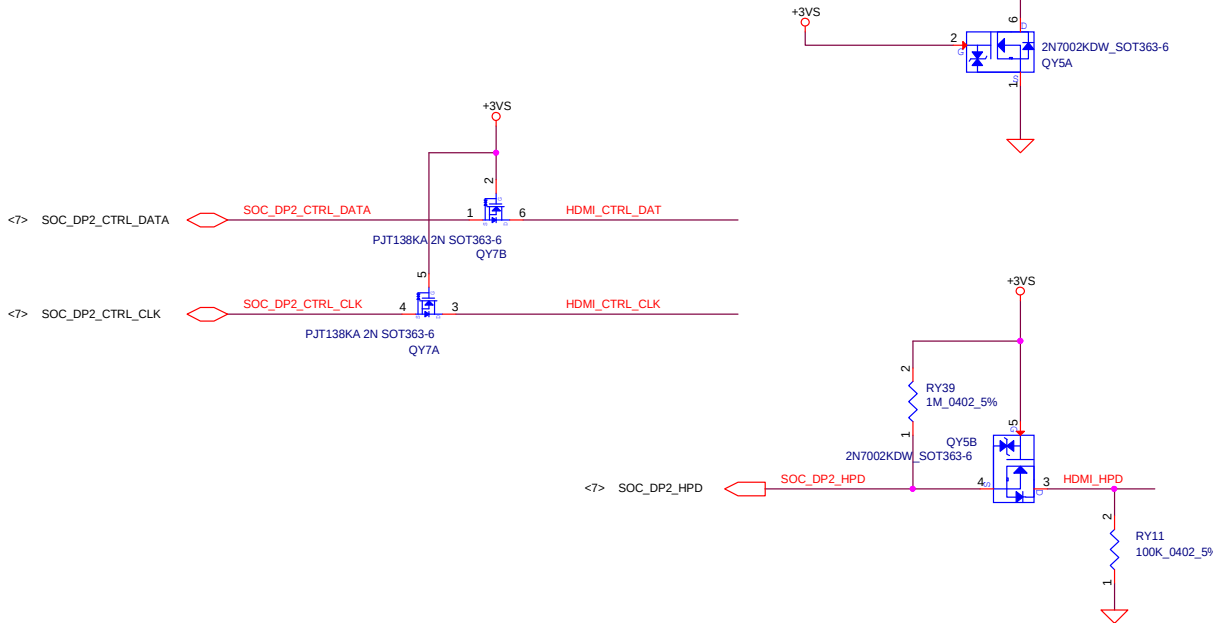
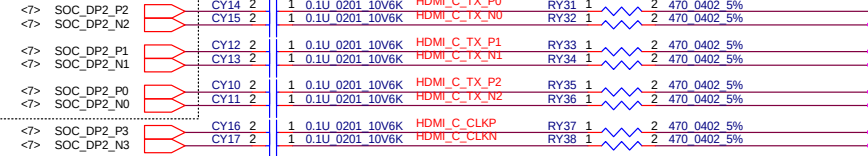
LED PANEL Conn.



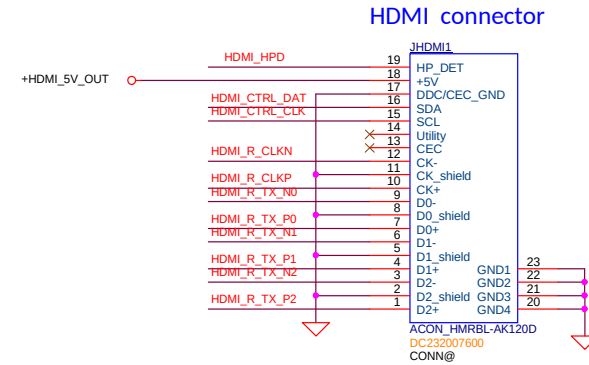
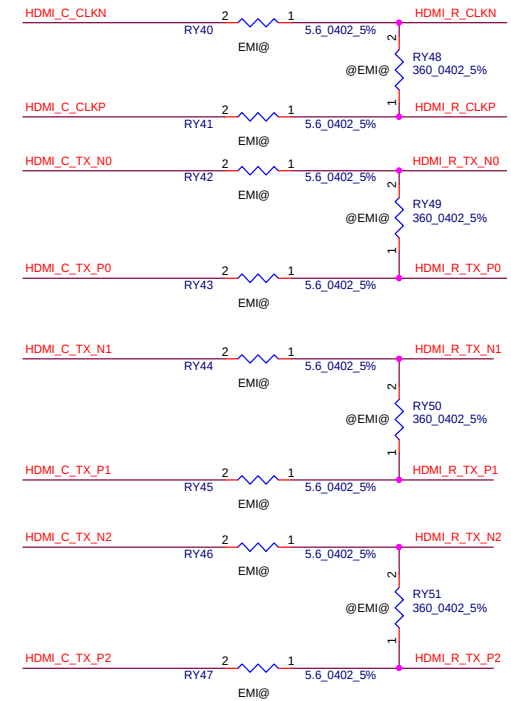
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| | | | | | | Size | | Document Number | | Rev | |
| | | | | | | Custom | | EH7LW M/B LA-H792P | | 0.1 | |
| | | | | | | Date: | | Thursday, June 06, 2019 | | Sheet 21 of 46 | |



port 0, 2 swap for INTEL HDMI



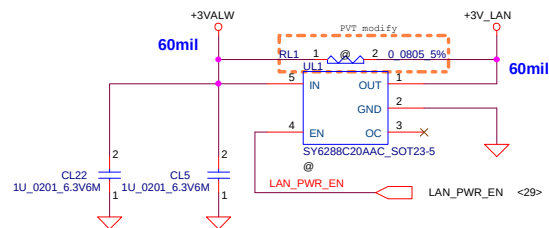
P/N: SC300001G00,S DIO(BR) AZC099-04S.R7G SOT23 ESD



SYMBOL: DC232004700

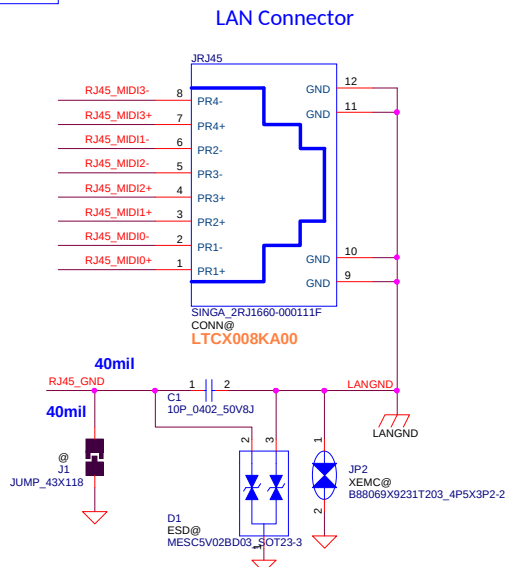
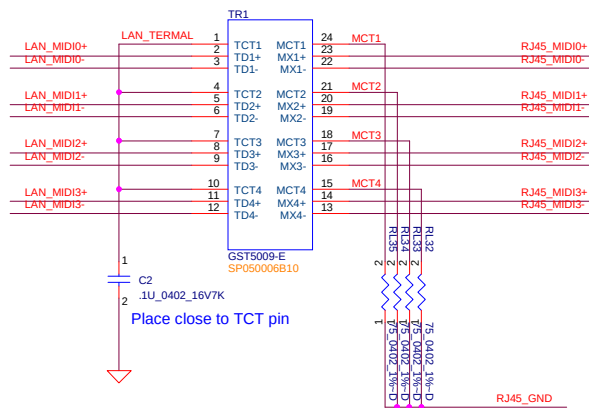
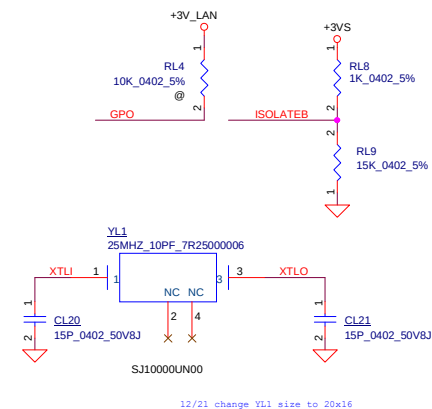
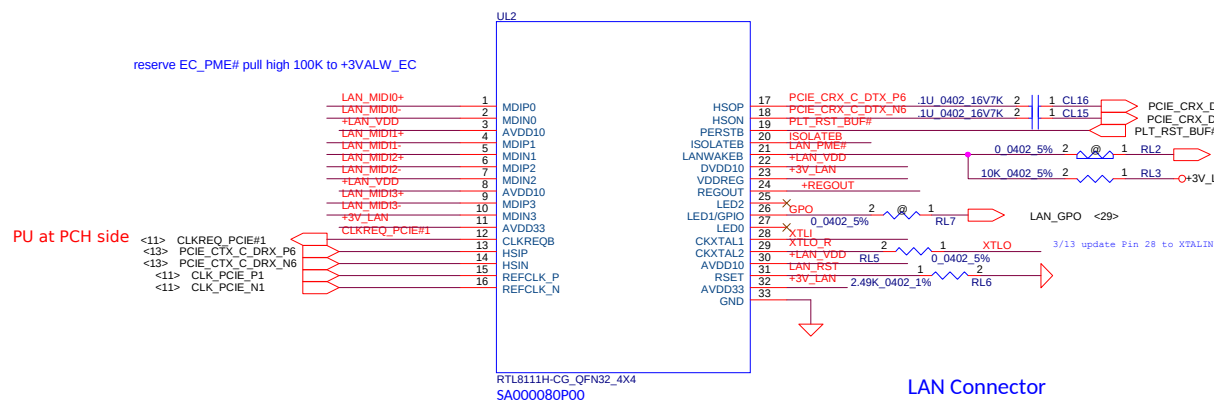
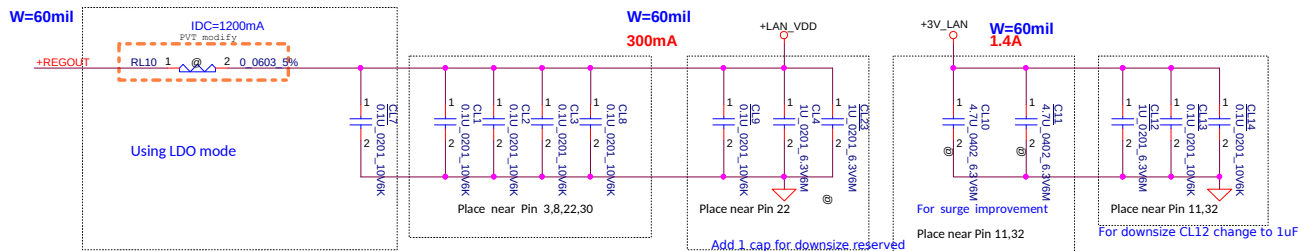
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| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
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| Size | Document Number | Rev | | 0.1 | |
| Date: | Thursday, June 06, 2019 | Sheet | 22 | of | 46 |

LAN-RTL8111H



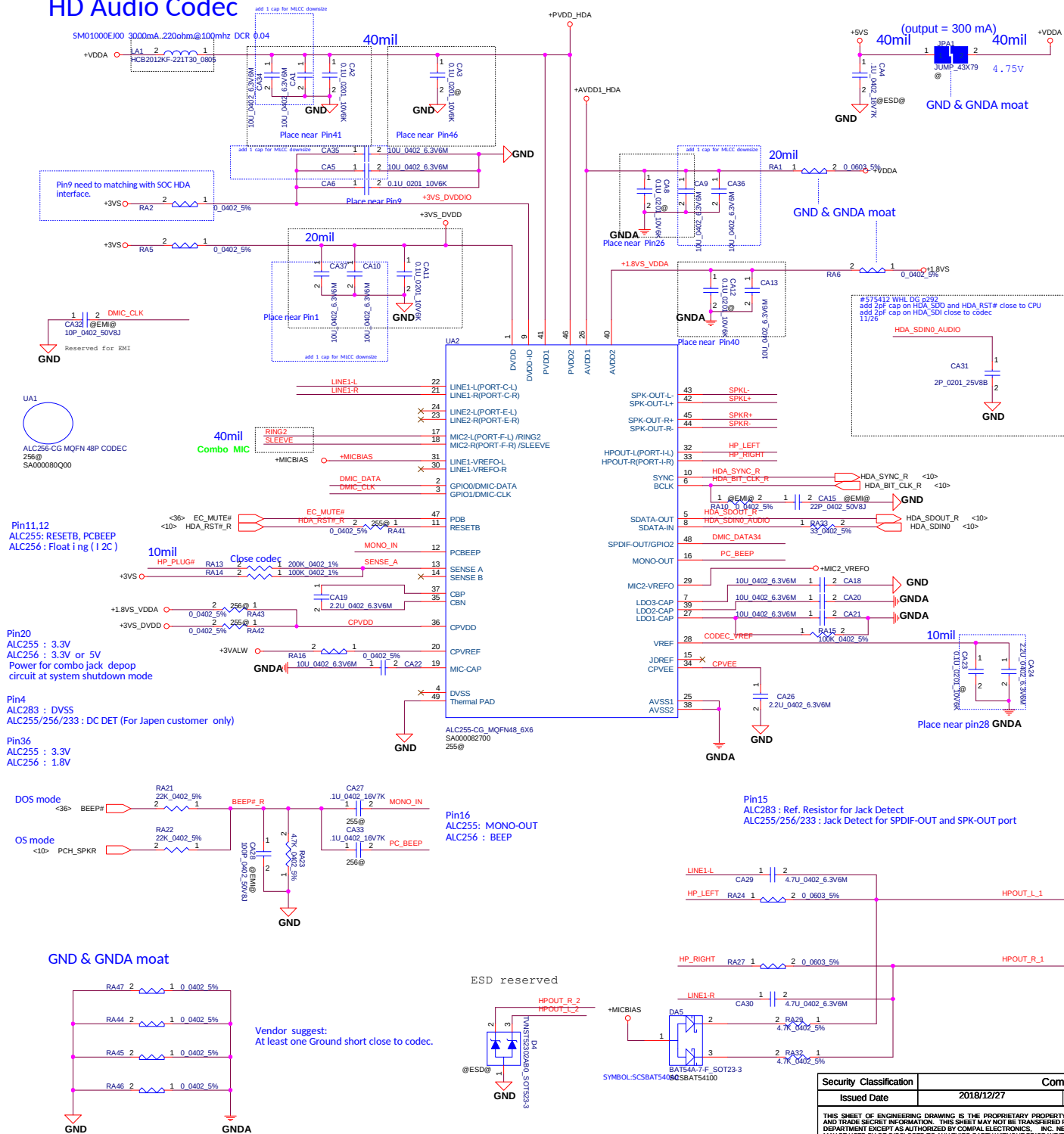
From EC

High active.
EN threshold voltage min:1.2V typ:1.6V max:2.0V
Current limit threshold 1.5~2.8A
+3V_LAN Rising time must >0.5 ms and <100 ms

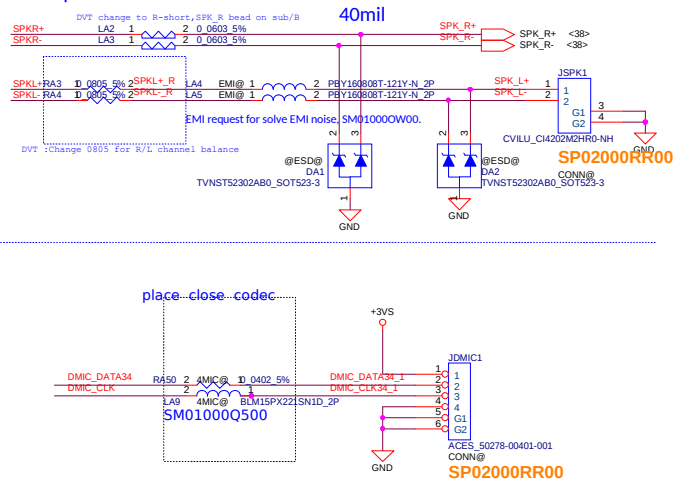


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| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | | | | | |
| Issued Date | | 2018/12/27 | Deciphered Date | | 2019/12/27 | Title | | | |
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| | | | | | | Size | Document Number | Rev 0.1 | |
| | | | | | | Custom | EH7LW M/B LA-H792P | | |
| | | | | | | Date: | Friday, August 02, 2019 | | Sheet |

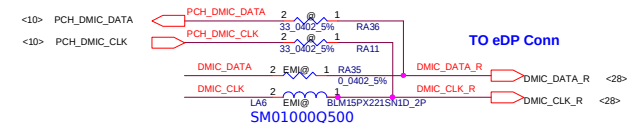
HD Audio Codec



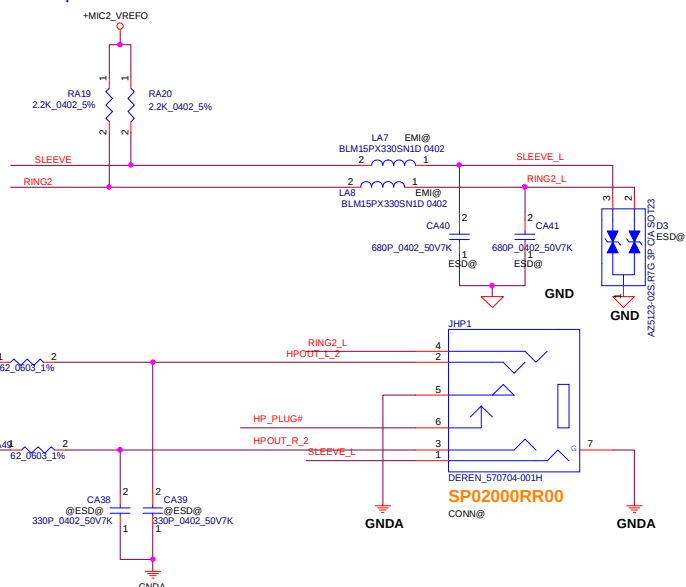
Int. Speaker Conn.



Digital MIC

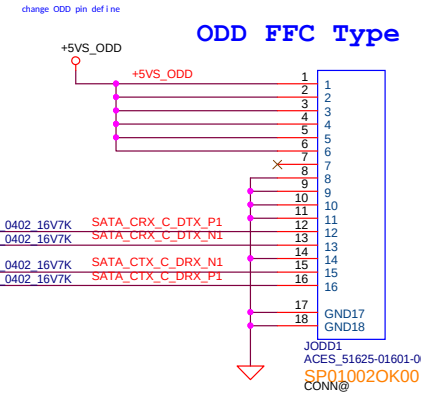
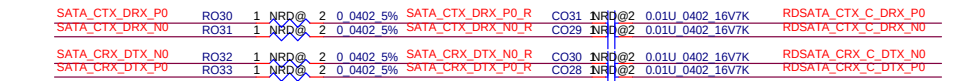
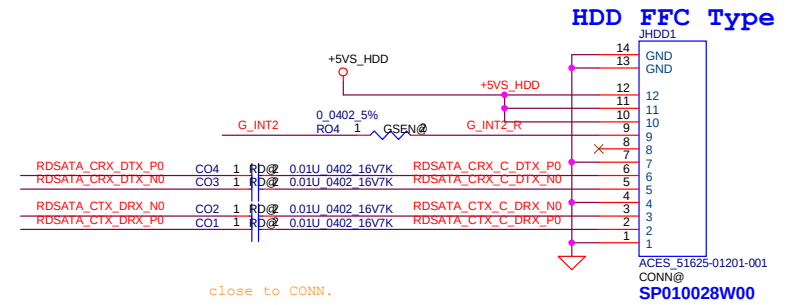
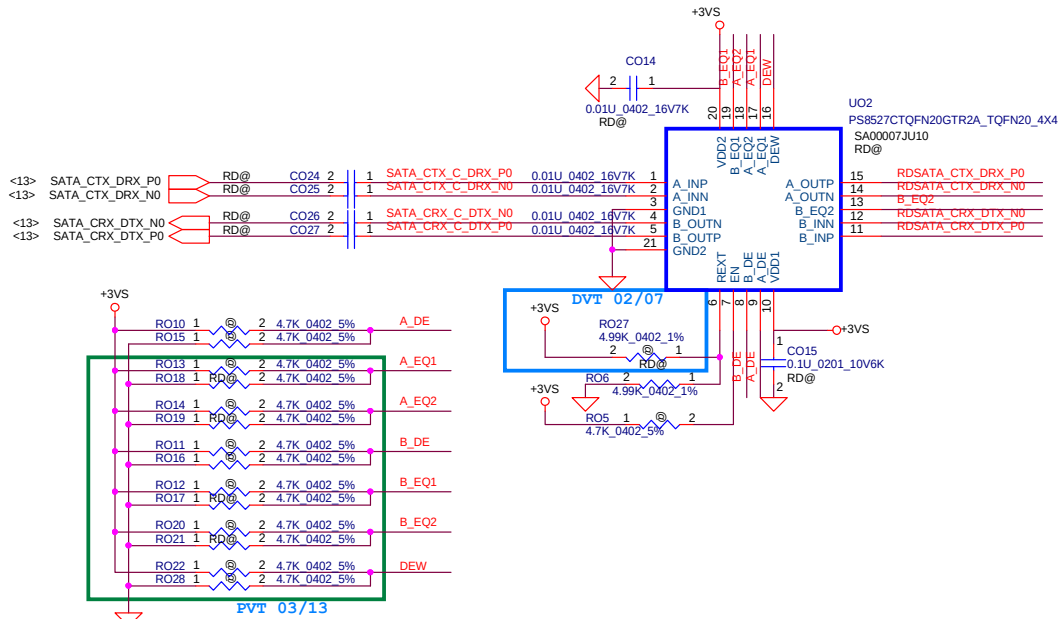
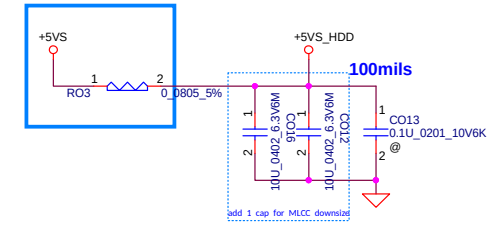
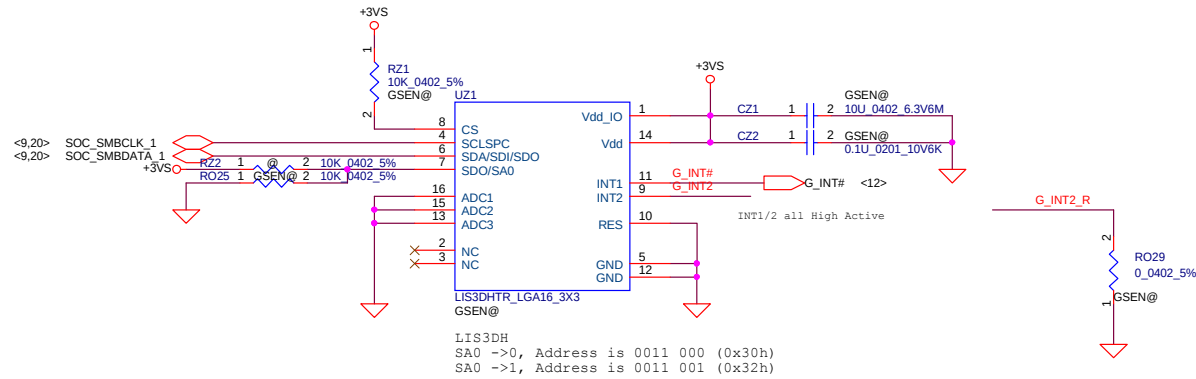


Headphone Out



| | | | | | | | | | | | | | |
|---|--|--------------------|--|-----------------|--|--------------------------|--|------------------------------------|--|-------|--|----------|--|
| Security Classification | | Compal Secret Data | | UNCLASSIFIED | | Compal Electronics, Inc. | | | | | | | |
| Issued Date | | 2018/12/27 | | Deciphered Date | | 2019/12/27 | | Title | | | | | |
| | | | | | | | | HD Audio Codec ALC255/ALC256 Colay | | | | | |
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| | | | | | | Custom | | EH7LW M/B LA-H792P | | | | 0.1 | |
| | | | | | | Date: | | Thursday, June 06, 2019 | | Sheet | | 25 of 46 | |

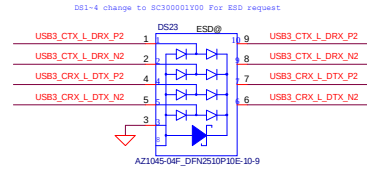
G-Sensor reserved for BA serial



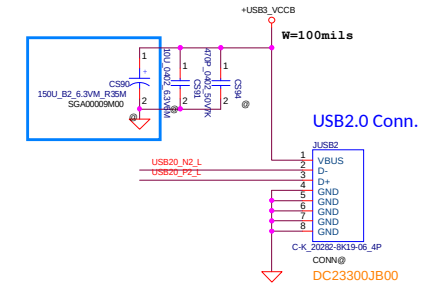
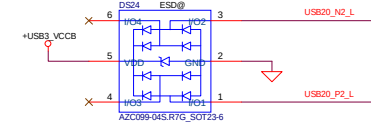
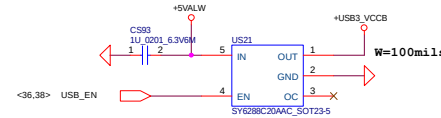
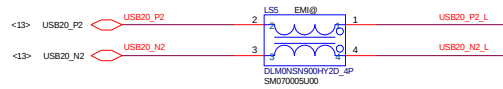
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|---|------------|--------------------|------------|--------------------------|-------------------------|----------------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | | |
| Issued Date | 2018/12/27 | Deciphered Date | 2019/12/27 | Title | G-Sensor/HDD/ODD | |
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| | | | | Custom | E7H7LW M/B LA-H792P | 0.1 |
| | | | | Date: | Thursday, June 06, 2019 | Sheet 26 of 46 |

USB3.0 (Port 2)

USB3 port reserved



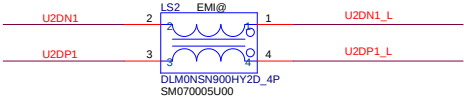
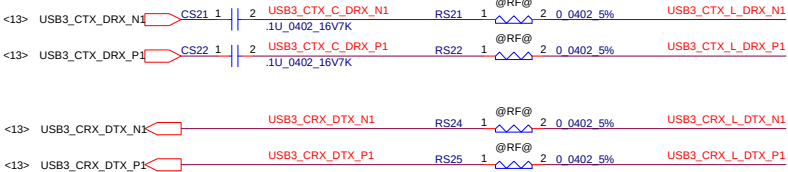
USB2.0 (Port 2)



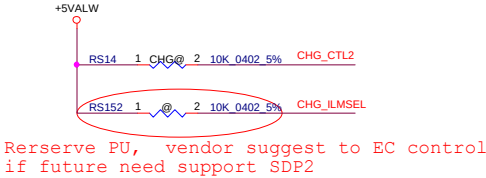
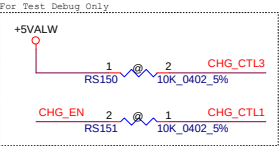
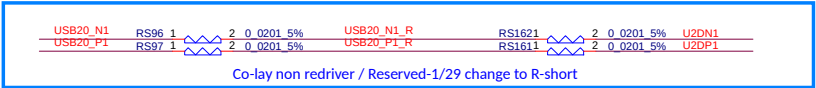
Symbol: DC23300N800
compatible: DC23300TT00

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| | | | | EH71W M/B LA-H792P |
| | | | | Rev 0.1 |
| | | | | Date: Thursday, June 06, 2019 |
| | | | | Sheet 27 of 46 |

USB3.0 (Port 1)

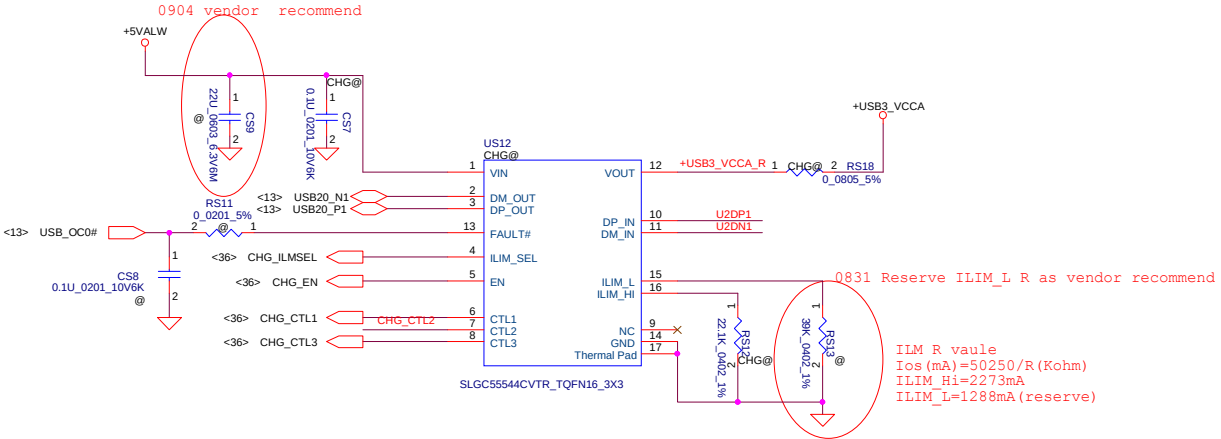
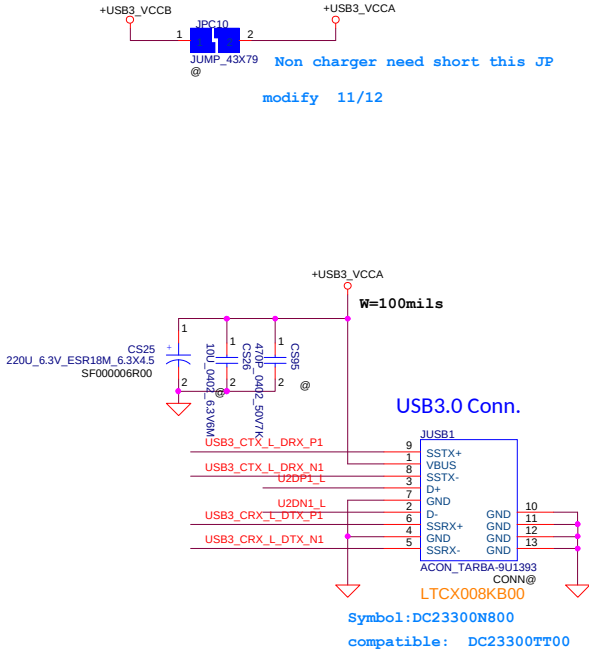
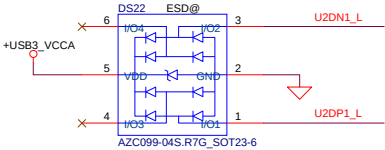
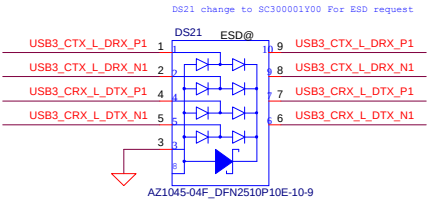


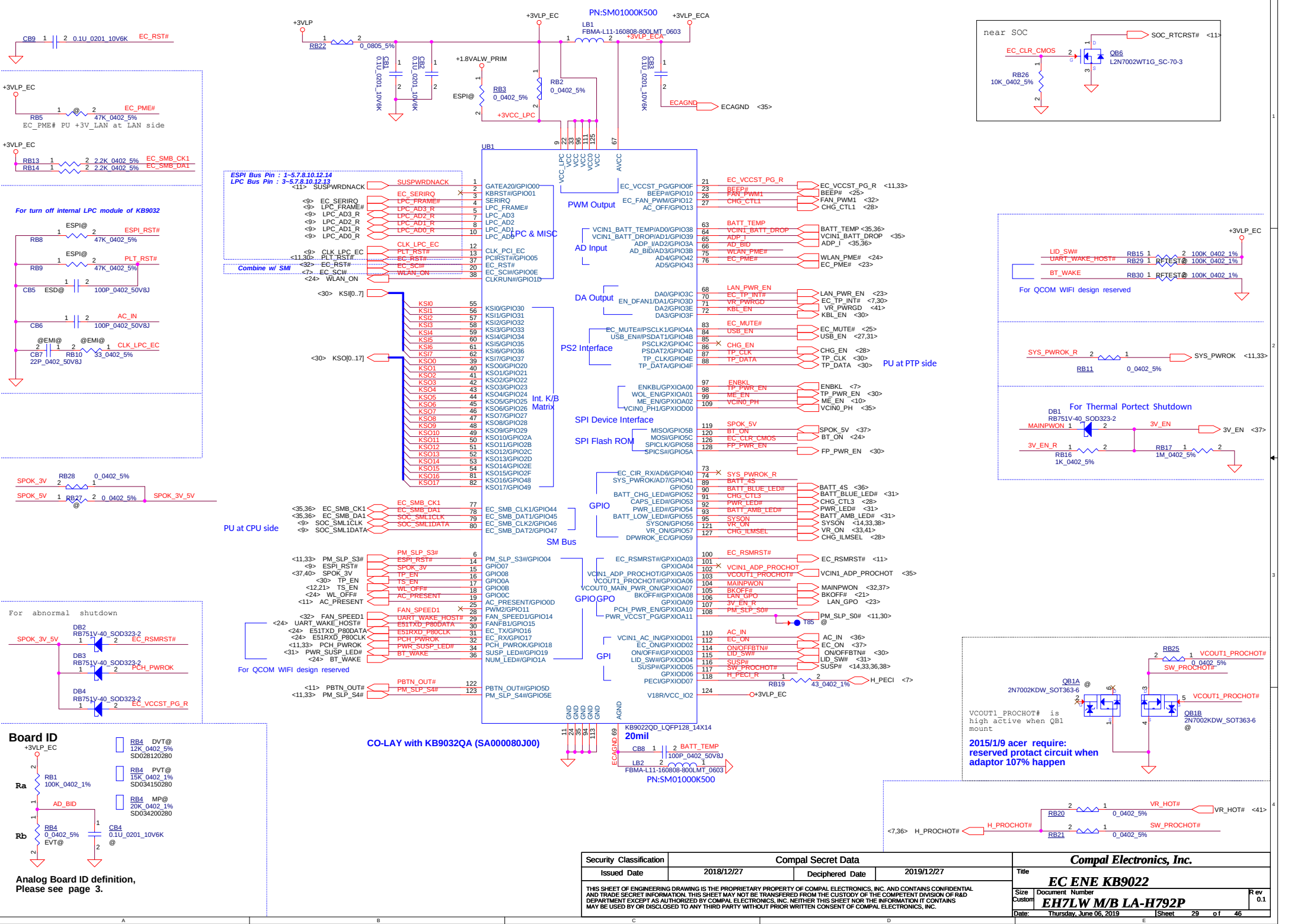
DVT: R-short



USB Host Charger Truth Table

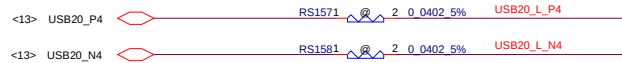
| CHG_EN | CTL1 | CTL2 | CTL3 | ILIM_SEL | MODE | Current Limit Setting | Note |
|--------|------|------|------|----------|----------|-----------------------|-------------------------|
| 0 | 0 | 1 | 0 | 1 | SDP1-OFF | ILIM_H | Port power off |
| 1 | 0 | 1 | 0 | 1 | SDP1 | ILIM_H | Data Lines Connected |
| 1 | 0 | 1 | 1 | 1 | DCP Auto | ILIM_H | Data Lines Disconnected |
| 1 | 1 | 1 | 1 | 1 | CDP | ILIM_H | Data Lines Connected |





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| Issued Date | 2018/12/27 | Deciphered Date | 2019/12/27 | Title | |
| | | | | EC ENE KB9022 | |
| | | | | Size | Document Number |
| | | | | Customer | EH7LW M/B LA-H792P |
| | | | | Date | Thursday, June 06, 2019 |
| | | | | Sheet | 29 of 46 |
| | | | | Rev | 0.1 |

USB2 I/O



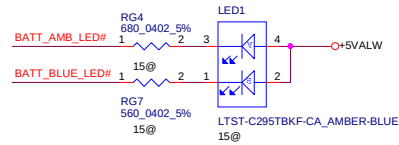
Card reader

Reserved CMC on SUB/B side

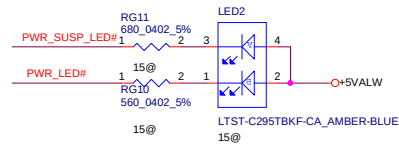


LED for 15" UMA

Battery LED



Power LED

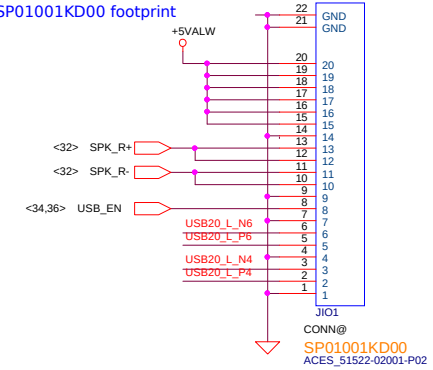


LID for 15" DIS

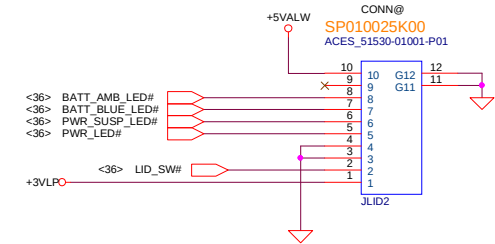
MB LID SW remove on UMA SKU

I/O Borad (USB2 /Card reader/ Speaker-RCH)

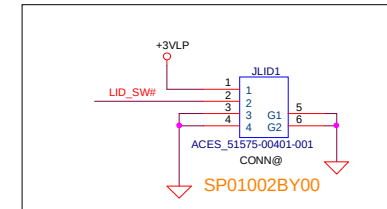
PVT:change to SP01001KD00 footprint



LID/B with LED for 17" UMA & DIS



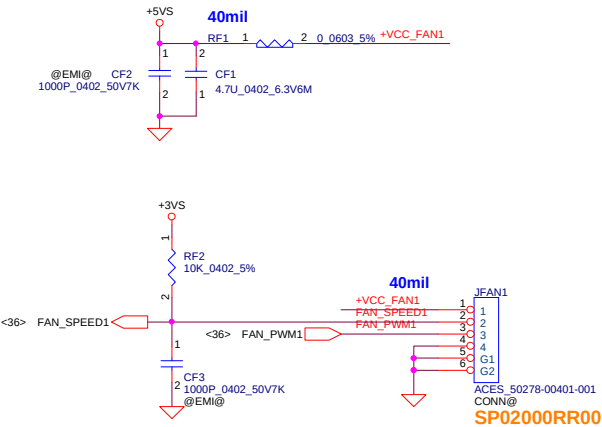
LID/B for 15" UMA 4pin



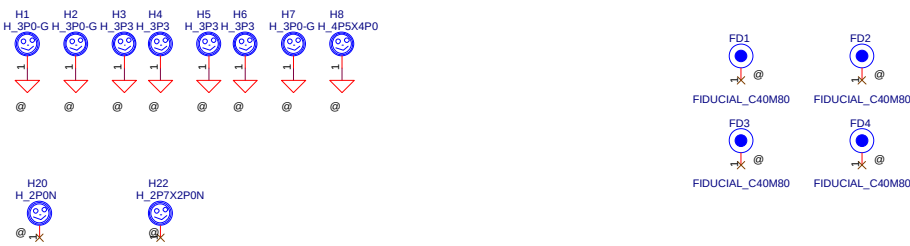
| Security Classification | | | | Compal Secret Data | | | | Compal Electronics, Inc. | | | |
|-------------------------|--|--|--|--------------------|--|-----------------|--|--------------------------|--|-------------------------------|--|
| Issued Date | | | | 2018/12/27 | | Deciphered Date | | 2019/12/27 | | Title | |
| | | | | | | | | | | IO/LID/LED | |
| | | | | | | | | | | Size Document Number | |
| | | | | | | | | | | EH7LW M/B LA-H792P | |
| | | | | | | | | | | Date: Thursday, June 06, 2019 | |
| | | | | | | | | | | Sheet 31 of 46 | |
| | | | | | | | | | | Rev 0.1 | |

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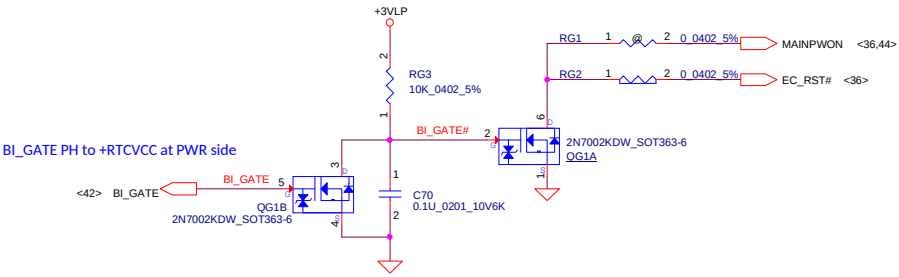
FAN1 Conn



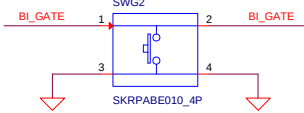
Screw Hole



Reset Circuit

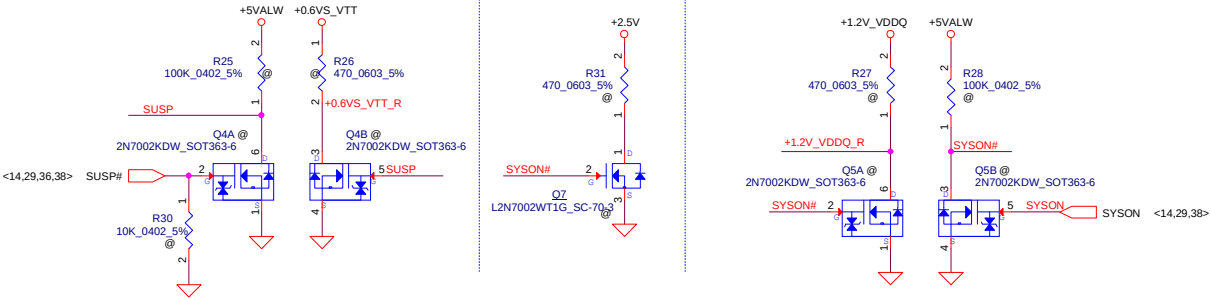
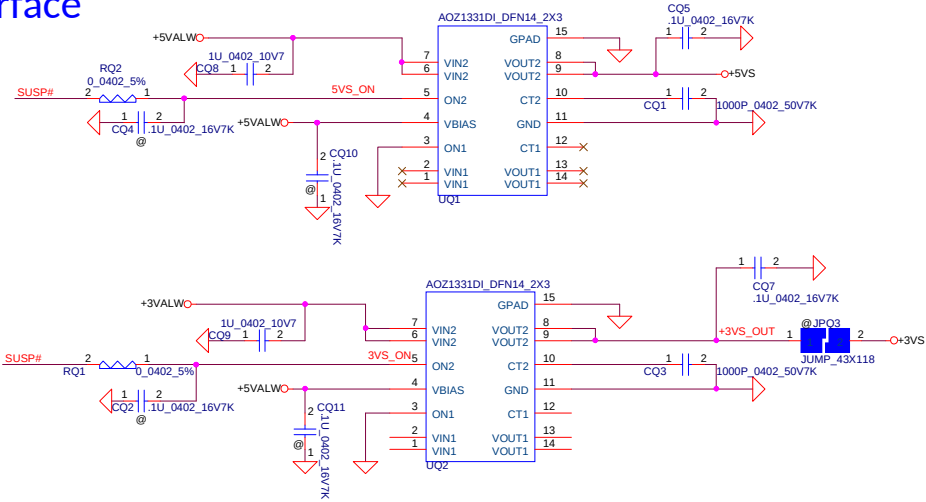


Reset Button

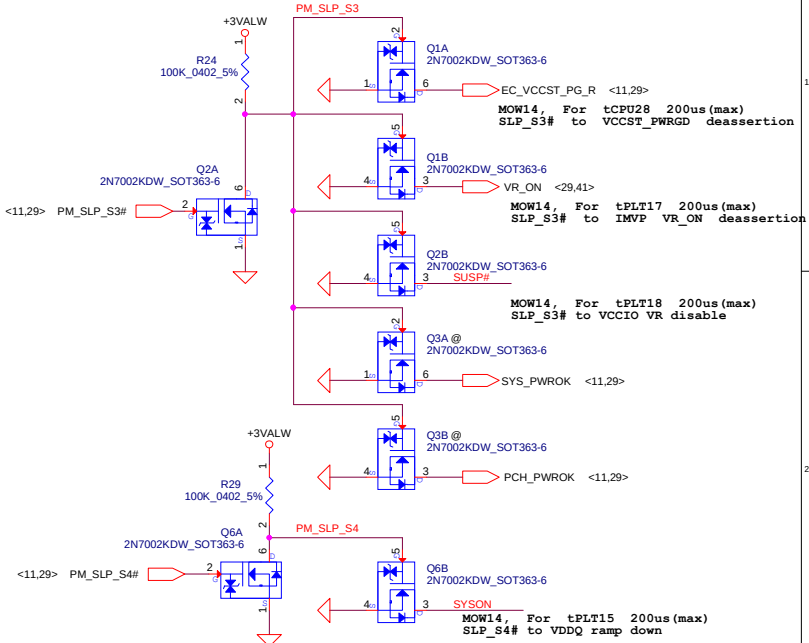


| | | | | | |
|---|--|--------------------------|--|--------------------------|--|
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| | | | | Document Number | |
| | | | | EH7LW M/B LA-H792P | |
| | | | | Date | |
| | | | | Thursday, June 06, 2019 | |
| | | | | Sheet | |
| | | | | 32 of 46 | |
| | | | | Rev | |
| | | | | 0.1 | |

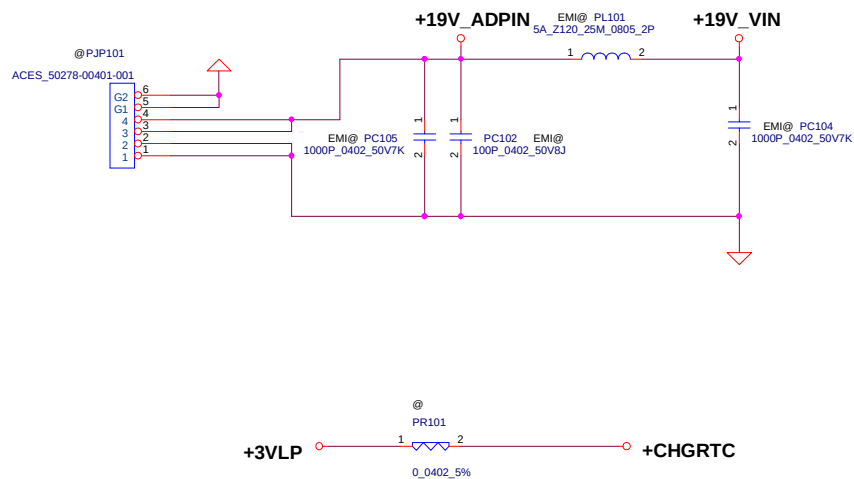
DC Interface



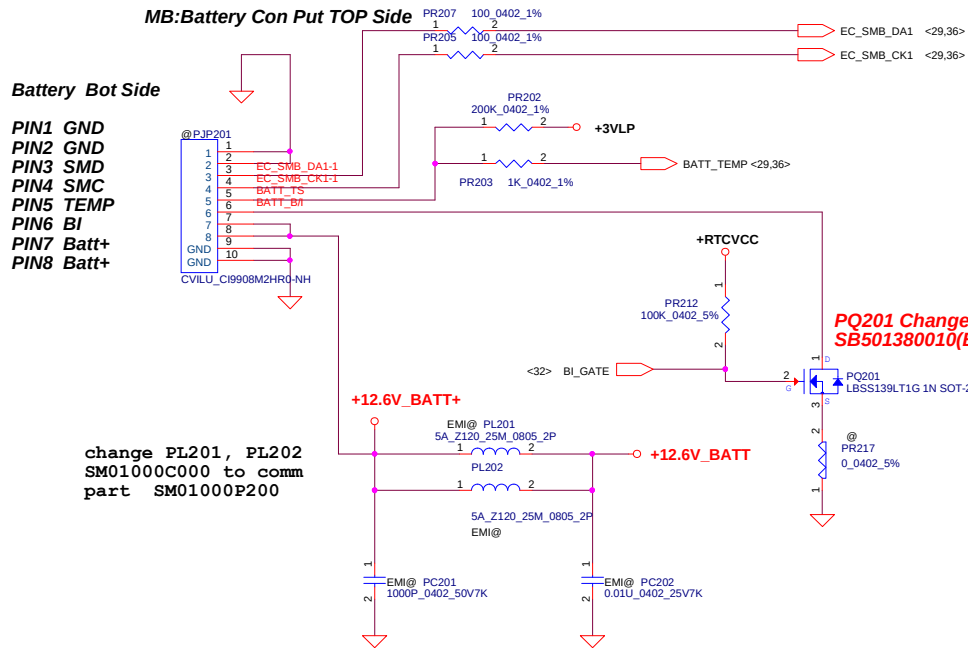
For Power ON/Off Sequence



| | | | | | | | | | | | |
|---|--|--------------------|--|-----------------|--|--------------------------|--|-------------------------|--|----------------|--|
| Security Classification | | Compal Secret Data | | | | Compal Electronics, Inc. | | | | | |
| Issued Date | | 2018/12/27 | | Deciphered Date | | 2019/12/27 | | Title | | | |
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| | | | | | | Size | | Document Number | | Rev | |
| | | | | | | Cust | | EH7LW M/B LA-H792P | | 0.1 | |
| | | | | | | Date: | | Thursday, June 06, 2019 | | Sheet 33 of 46 | |

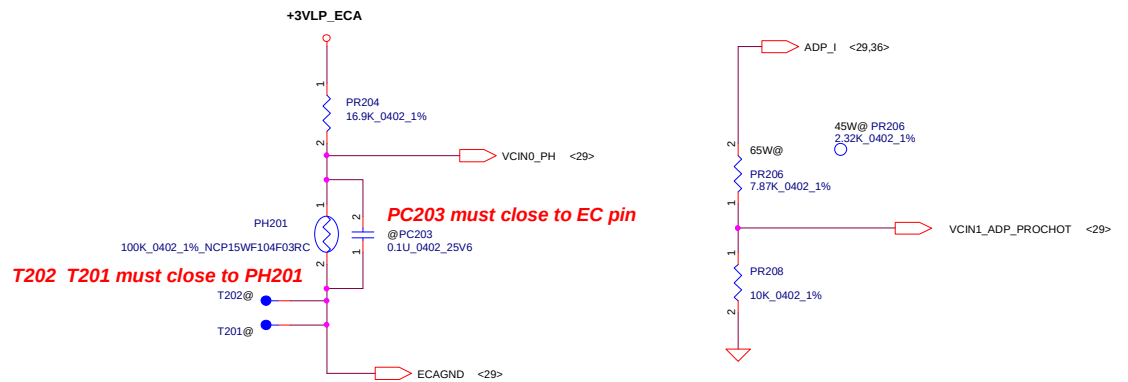
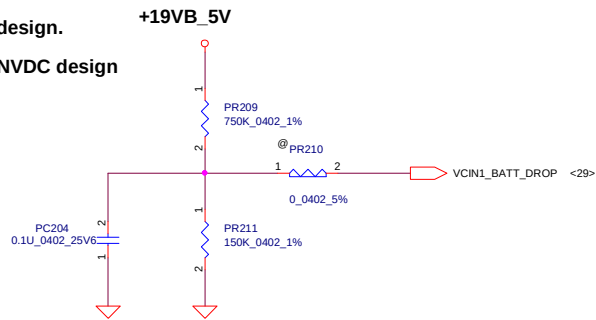


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| Issued Date | 2018/12/27 | Deciphered Date | 2019/12/27 | Title | |
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| | | | | Size | Rev |
| | | | | Custom | 0.1 |
| Date: Thursday, June 06, 2019 | | Sheet 34 of 46 | | E | |



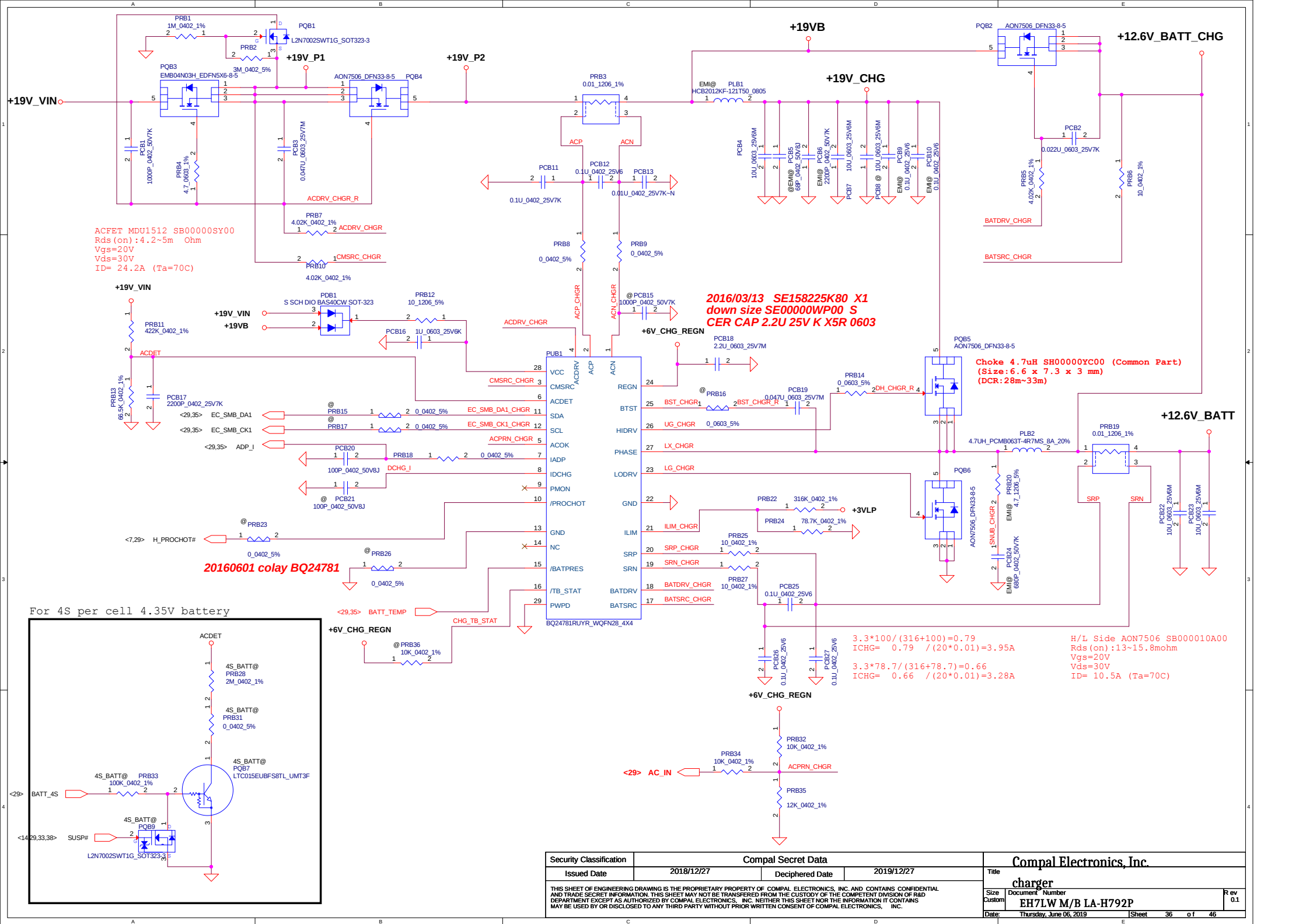
2013/06/07
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

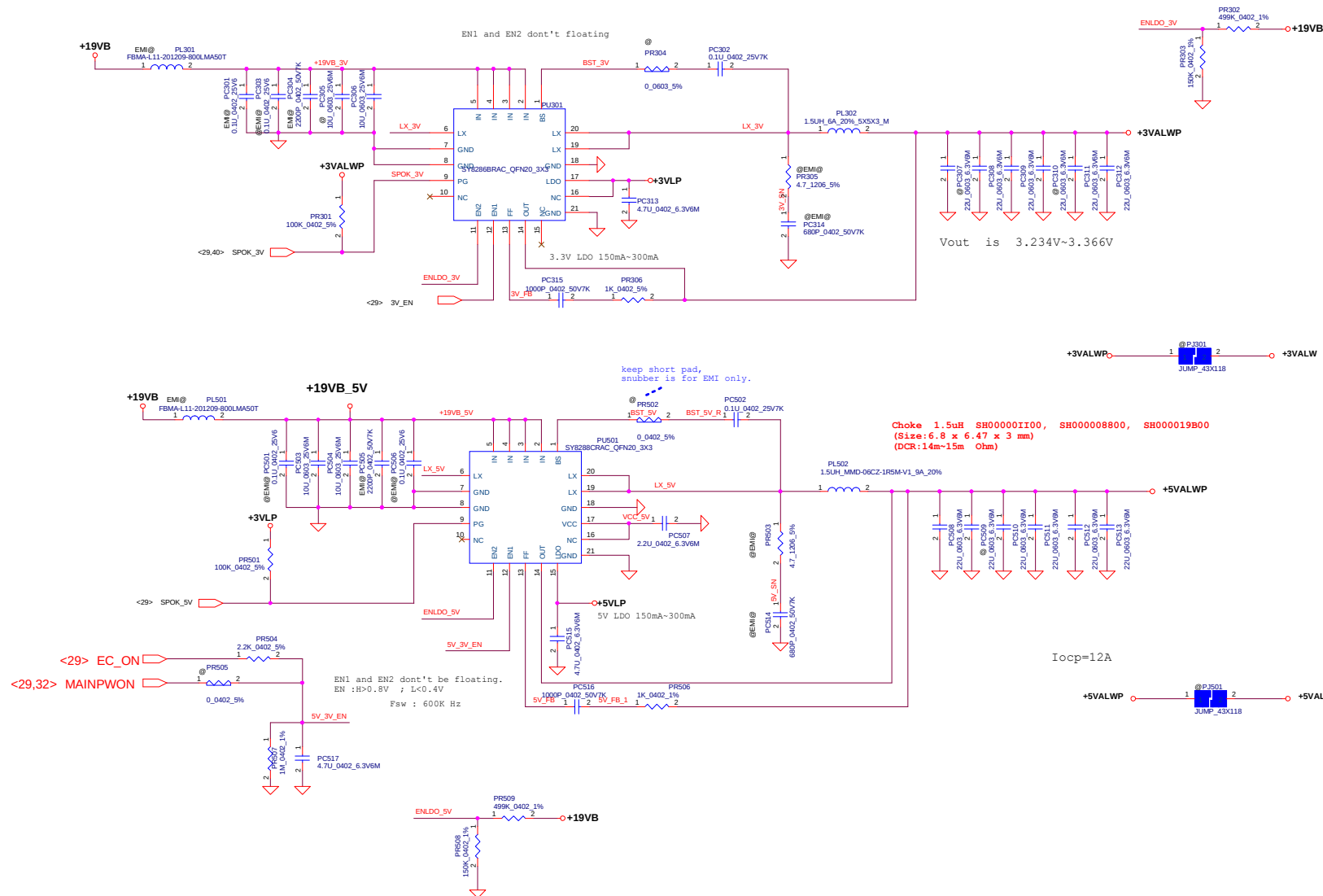
VAL50/ZAL20 Battery is 3-cell NVDC design.
B+=9V
Change PR12=50k if Battery is 2-cell NVDC design
B+=6V



PH1 under CPU botten side :
CPU thermal protection at 89 +-3 degree C
Recovery at 56 +-3 degree C

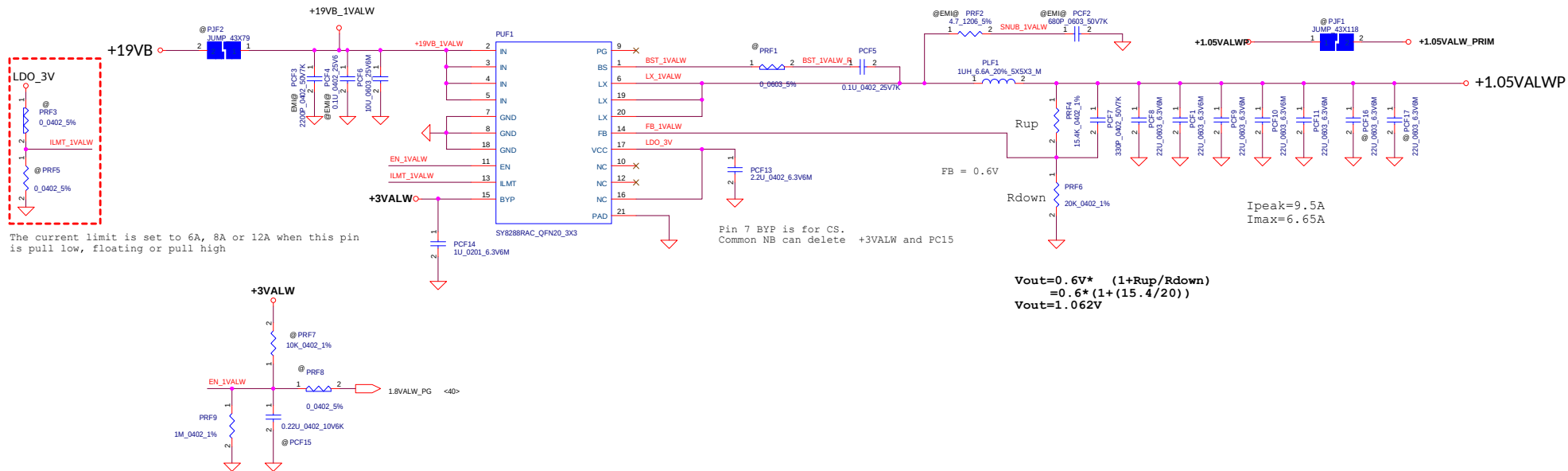
| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. | |
|---|--------------------|-----------------|------------|---------------------------------|---------------------------------------|
| Issued Date | 2018/12/27 | Deciphered Date | 2019/12/27 | Title | |
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| | | | | Size Custom | Document Number EH7LW M/B LA-H792P |
| | | | | Date Thursday, June 06, 2019 | Rev 0.1 |
| | | | | Sheet | 46 |



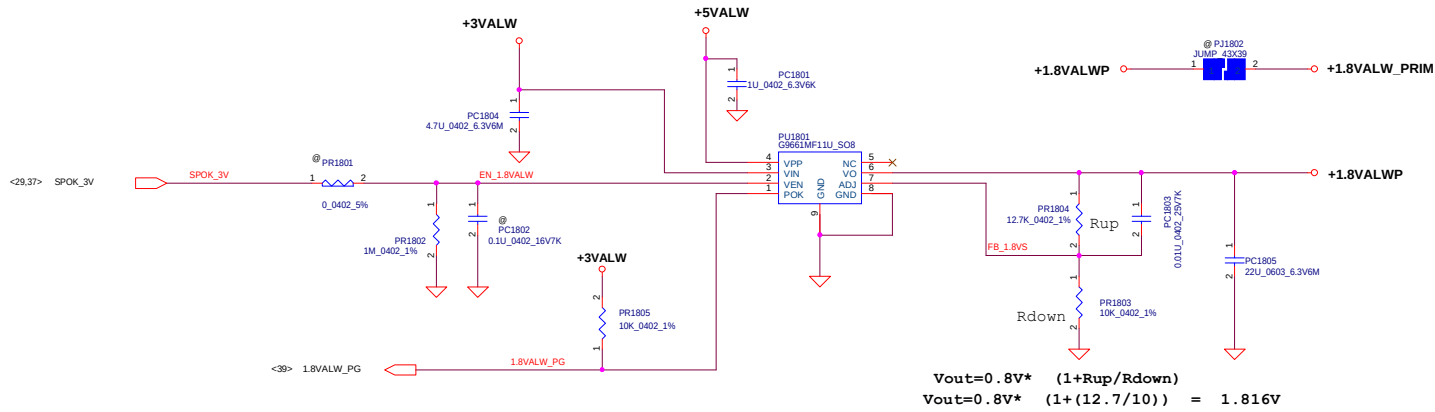


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|---|------------|--------------------|------------|--------------------------|-------------------------|
| Issued Date | 2018/12/27 | Deciphered Date | 2019/12/27 | Title | +3VALW/+5VALW |
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| | | | | Custom | EH7LW M/B LA-H792P |
| | | | | Date: | Thursday, June 06, 2019 |
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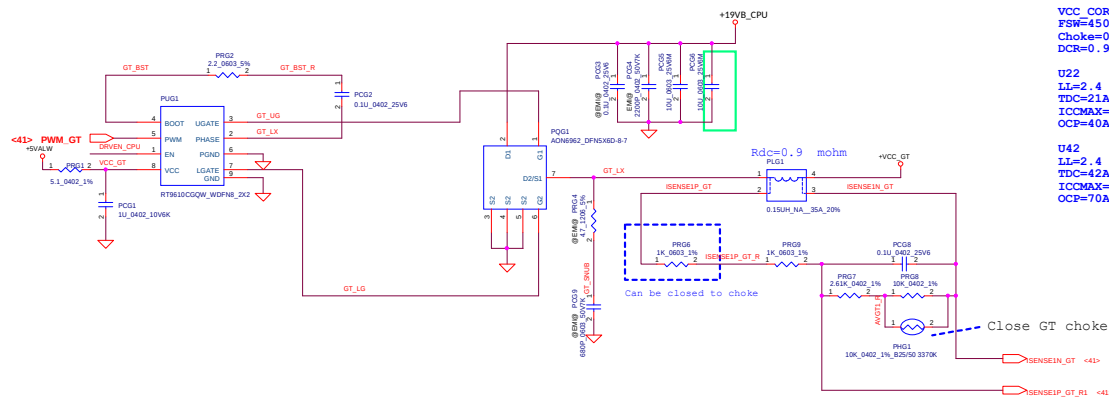
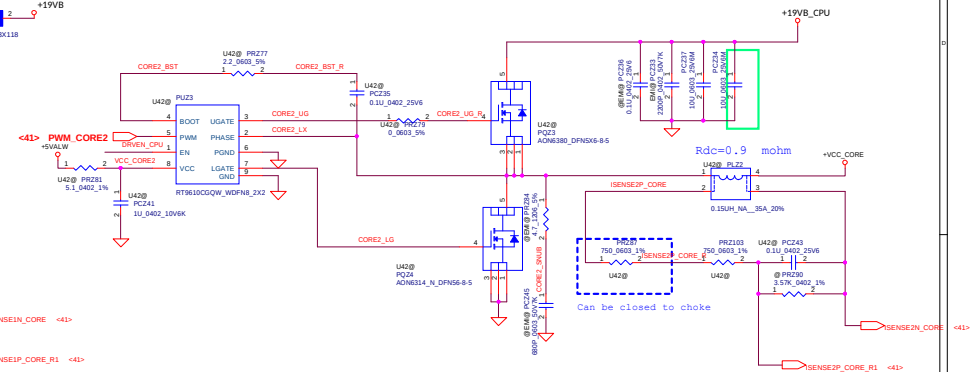
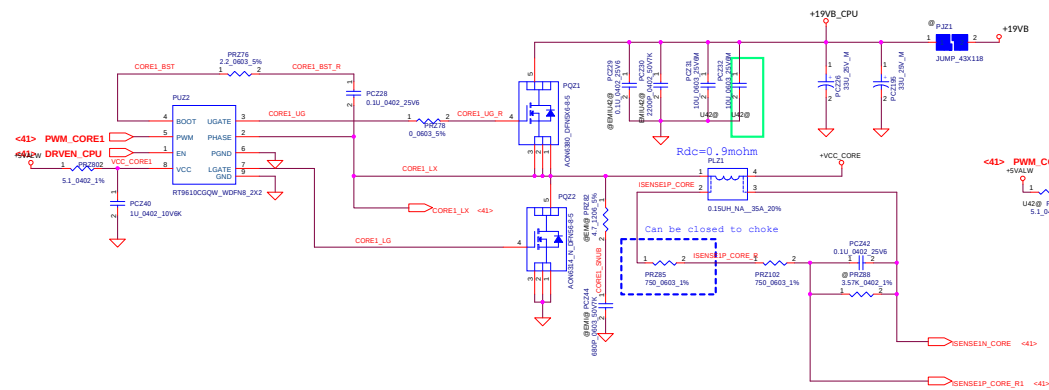
EN pin don't floating
If have pull down resistor at HW side, pls delete PR702



| | | | | | |
|---|--------------------|-----------------|------------|--------------------------|-------------------------|
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| | | | | C | EH7LW M/B LA-H792P |
| | | | | Date | Thursday, June 06, 2019 |
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|---|--------------------|-----------------|------------|--------------------------|-------------------------|
| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. | |
| Issued Date | 2018/12/27 | Deciphered Date | 2019/12/27 | Title | SY8032 |
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| | | | | C | EH7LW M/B LA-H792P |
| | | | | Date: | Thursday, June 06, 2019 |
| | | | | Sheet | 40 of 46 |
| | | | | Rev | 0.1 |



VCC_CORE
FSW=450kHz
Choke=0.15uH
DCR=0.9mohm +/- 5%

VCC_GT
FSW=450kHz
Choke=0.15uH
DCR=0.9mohm +/- 5%

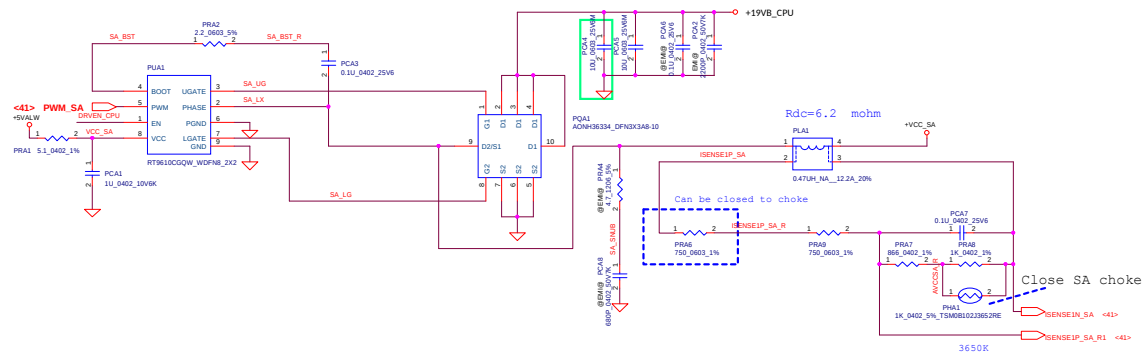
VCC_SA
FSW=600kHz
DCR=6.2mohm +/- 5%

U22
LI=2.4mohm
TDC=21A
ICCMAX=32A
OCP=40A

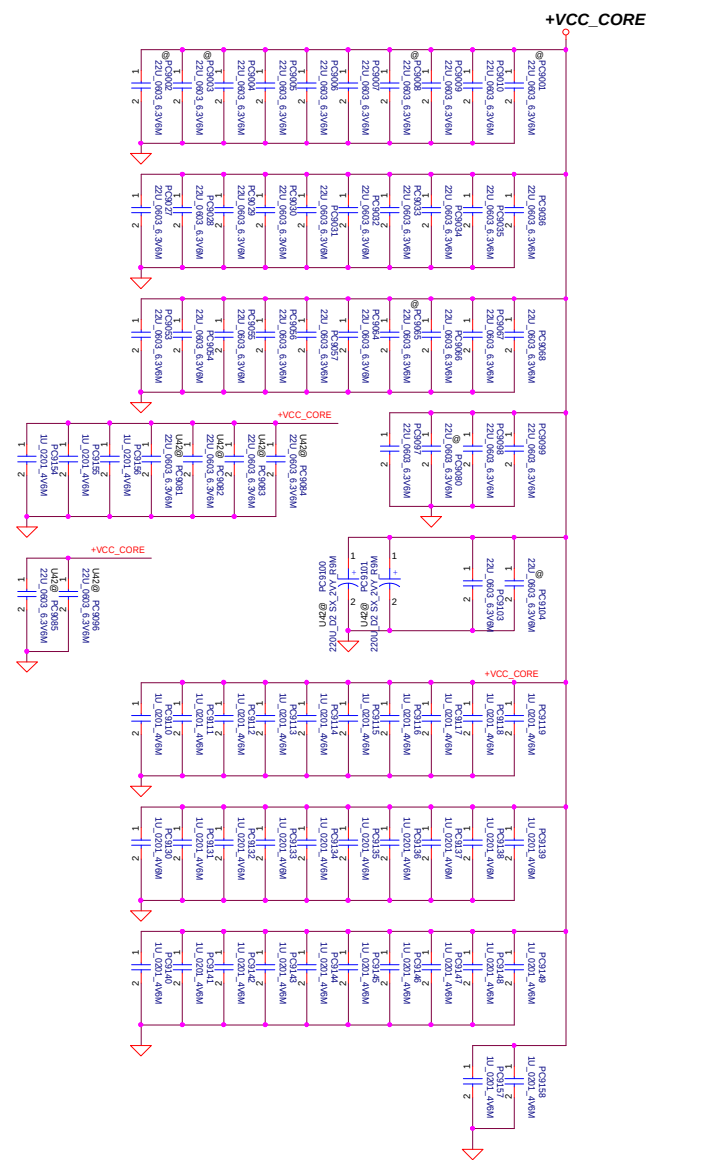
U42
LI=2.4mohm
TDC=42A
ICCMAX=64A
OCP=70A

U22
LI=10.3mohm
TDC=4A
ICCMAX=4.5A
OCP=9.5A

U42
LI=10.3mohm
TDC=6A
ICCMAX=6A
OCP=9.5A

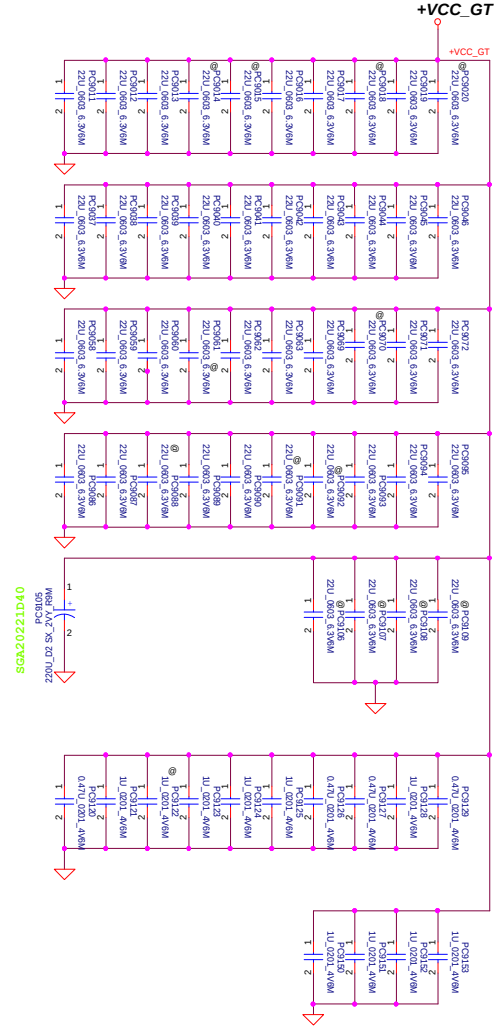


| | | |
|-------------------------|-------------------------|--------------------------|
| Security Classification | Compel Secret Data | Compel Electronics, Inc. |
| Issued Date | 2018/12/27 | Deciphered Date |
| Deciphered Date | 2019/12/27 | |
| Title | CPU Power stage | |
| Size | EH7LWM/B1A-H792P | Rev |
| Docu | 0.1 | |
| Date | Thursday, June 06, 2019 | Sheet |
| | 42 | 48 |

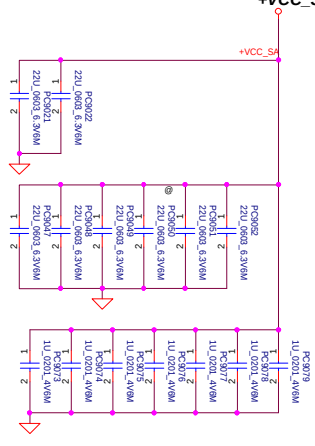


2017/07/03
 VCore Output Capacitor:
 U42
 22uF_0603*35
 1uF_0201*35
 220uF*2
 UNPOP
 22_0603*7
 220uF*2

2017/07/03
 VCore Output Capacitor:
 U22
 22uF_0603*29
 1uF_0201*35
 UNPOP
 22_0603*7
 220uF*2



220uF*1
 22uF*31
 1uF*9
 0.47uF*4
 unpop:
 22uF*13
 1uF*1



SA
 pop:
 22uF_0603*7
 1uF_0201*7
 unpop:
 22uF_0603*1

| | | | | | |
|---|------------|--------------------|------------|--------------------------|-------------------------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2018/12/27 | Deciphered Date | 2019/12/27 | Title | Power Train |
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| | | | | Date | Thursday, June 06, 2019 |
| | | | | Sheet | 43 of 46 |
| | | | | Rev | 01 |

HW Schematic chang list (P.I.R)

| Date | Rev. | Modify Item | Date | Rev. | Modify Item |
|------|------|--|------|------|-------------|
| 1/22 | 0.1 | Add cnvi cap(CM4) as intel request update JIO1/JFP1 pin define Add UART routing for RF test | | | |
| 1/29 | 0.1 | update JIO1 pin define change 0-ohm to R-short remove SWK1/UG1/UG2/JPQ2 | | | |
| 2/12 | 0.1 | change RA3/RA4 to 0805 size | | | |
| 3/13 | 1.0 | Add DA3/DA4 for audio ESD protection | | | |
| 3/15 | 1.0 | change JIO1 footprint update UL2 pin28/pin29 pin define Delete JC1 ROM socket change 0-ohm to R-short | | | |
| 5/9 | 1A | update RC262 75k for CML | | | |

HW Schematic chang list (P.I.R)

| Item | Page | Date | Rev. | Reason for change | Modify Item |
|------|------|------|------|-------------------|-------------|
|------|------|------|------|-------------------|-------------|

| | | | | | |
|---|--|-------------------------|-----------------|-----------------|--|
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| | | | | Document Number | |
| | | | | Rev | |
| | | | | 0.1 | |
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Version change list (P.I.R. List)

Page 1 of 1 for
PWR

| Item | Fixed Issue | Reason for change | Rev. | PG# | Modify List | Date | Phase |
|------|-----------------------------|---|------|---------|--|---------|--------|
| 01 | change PL502 to common part | change PL502 to common part | | P.44 | change PL502 to common part(SH000016700) | 19.0212 | DVT |
| 02 | change CAP size to 0402 | change CAP size to 0402 for cost down | | P.43,44 | change PC302,PC502,PCB11 to SE00000W210 change PCB1 to SE074102K80 | 19.0212 | DVT |
| 03 | change 0 ohm to R-short | change 0 ohm to R-short for cost down | | | change PR101,PR217,PR210,PRB15,PRB17,PRB23,PRB26,PRB16,PR304,PR505,PR502,PRM8,PRM11,PRM12,PRF3,PRF8,PRF1,PR1801,PRZ15,PRZ94,PRZ47,PRZ95,PRZ50,PRZ93,PRZ25 to R-short (25PCS) | 19.0212 | DVT |
| 04 | DDR sequence | change PRM8 to 48.7K and PCM18 to 0.1u for sequence | | P.38 | change PRM8 to SD034487280 change PCM18 to SE102104K00 | 19.0215 | DVT |
| 05 | CPU transient | change R and C value for CPU transient test | | P.48 | change PCZ11 to 330PuF(SE074331K80) change PRZ45 to 63.4k ohm(SD03463K280)(U42) change PRZ49 to 5.49k ohm(SD034549180) | 19.0218 | DVT |
| 06 | DDR sequence | change PRM8 to 0 ohm and del PCM18 for sequence | | P.38 | change PRM8 to SD028000080 del PCM18 | 19.0328 | PVT |
| 07 | VR thermal alert adjust | change protect from 100c to 110c | | P.41 | change PHZ2,PHZ3 to SL200002I00, change PRZ51,PRZ66 to SD000000680, change PRZ52,PRZ69 to SD034332280, change PRZ67 to SD000000W580,change PRZ63 to SD034130280, change PRZ70 to SD034137180,change PRZ68 to SD034392180, change PRZ64 to SD034976180,change PRZ71 to SD00000W580,change PRZ74 to SD034165280 | 19.0507 | pre MP |
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